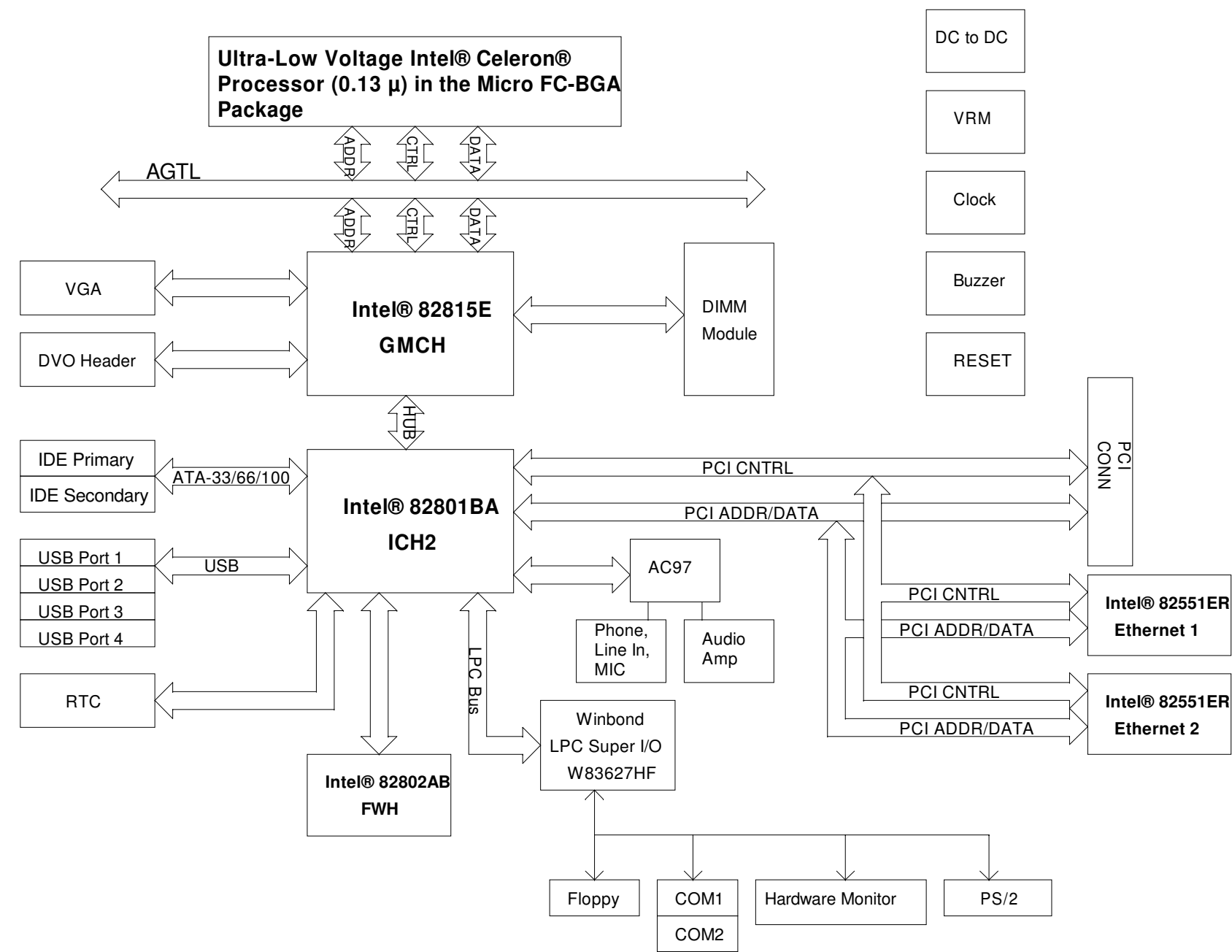


Intel® 815E Entry Appliance Platform  
Block Diagram



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CA = Communications Appliance Only  
IC = Interactive Client Only

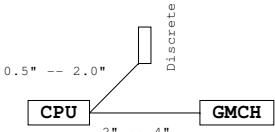
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| Title<br>BLOCK DIAGRAM  |   |            |
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General Board Design Requirements

- >> Board material shall be FR-4.
- >> Right angle traces shall not be used.
- >> Vias for decoupling capacitors shall be kept as close as possible to the capacitor pad.
- >> Trace impedance shall be 60 ohms, +/- 15%
- >> Total board thickness shall be .062".
- >> GND layers shall not be split.
- >> Top and bottom (outer) layers shall be no less than 1/2 oz copper before plating, inner layers shall be 1 oz copper.
- >> Series terminating resistors shall be kept as close to the driving pin as possible.
- >> Daisy chain signals going to more than one point shall not use stubs.
- >> Unless otherwise noted, all signal traces shall be between 5 and 6 mil width.
- >> Unless otherwise noted, minimum space between traces shall be 10 mils, including adjacent layers.
- >> One registration target shall be included on each corner of the board.
- >> Other specific routing requirements are included throughout schematic sheets.

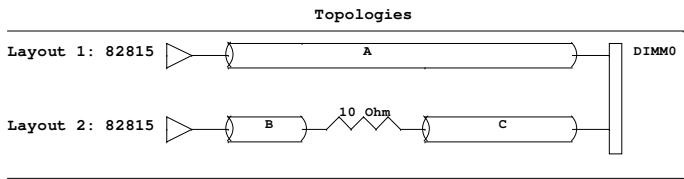
CPU Routing Requirements

- >> Route all GTL traces between CPU and GMCH as shown in the diagram to the right.
- >> Route all traces between CPU and GMCH on a layer adjacent to a ground plane, without layer changes.
- >> Minimum space between traces shall be 10 mils (unless otherwise noted); this includes adjacent signal layers.
- >> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing shall be less than 250 mils.
- >> The following signals require 25 mil spacing from other traces, including adjacent layers:
  - HA#[31:3], HD#[63:0], BREQ#0, HADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, A20M#, IGNNE#, INIT#, INTR, NMI, PWR\_OK\_2P5, SMI#, CPUSLP#, STPCLK#, 66#/100SEL,100#/133SEL,FERR#,CPURST#, HREQ#[4:0], RS#[2:0], GTLREF[7:0], PLL[2:1], (CPU\_TCK/TMS/TDI/TDO/TRST#, PRDY#, PREQ#).
- >> AGTL signals shall be well isolated from system memory signals. AGTL signal trace edges shall be at least 30 mils from system memory trace edges within 100 mils of the ball of the 82815 GMCH.
- >> Route GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.
- >> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.



Memory Bus Routing Requirements

- >> Minimum space between memory traces and other types of traces is 30 mils, including adjacent signal layers.
- >> Memory address, data, and control lines shall be routed as separate groups and treated as different signal types.

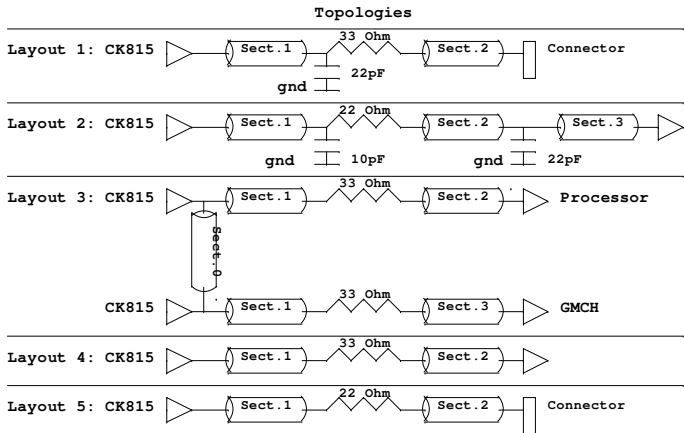


Routing Solution :

| Signal                          | Topologies | Width (mils) | Spacing (mils) | A (inches) | B (inches) | C (inches) |
|---------------------------------|------------|--------------|----------------|------------|------------|------------|
| SM_CSA#[1..0]                   | Layout 1   | 5            | 10             | 1-4.5      |            |            |
| SM_MAA[7:4]                     | Layout 2   | 10           | 10             |            | 0.4-0.5    | 2-4        |
| SM_CKE[1:0]                     | Layout 1   | 10           | 10             | 3-4        |            |            |
| SM_MD[63:0]                     | Layout 1   | 5            | 10             | 1.75-4     |            |            |
| SM_DQMA[7:0]                    | Layout 1   | 10           | 10             | 1.5-3.5    |            |            |
| SM_CAS#, SM_RAS#, SM_WE#        | Layout 1   | 10           | 10             | 1-4.0      |            |            |
| SM_BS[1:0], SM_MAA[12:8], [3:0] | Layout 1   | 10           | 10             | 1-4.0      |            |            |

Clock Routing Requirements

- >> Clock traces shall not alternate layers.
- >> All clocks shall be routed 5 mils wide with 15 mil spacing to any other signals.
- >> It is recommended to place capacitor sites within 0.5 inches of the receiver of all clocks. They are useful in system debug and AC tuning.
- >> Series resistor for clock guidelines: 22 ohm for GMCH SCLK and SDRAM clocks. All other clocks use 33 ohm.
- >> Each DIMM clock shall be matched within ±10 mils.



Routing Solution :

| Destination                   | Topologies | Sect.0 | Sect.1   | Sect.2          | Sect.3 |
|-------------------------------|------------|--------|----------|-----------------|--------|
| MEMCLK[3..0]                  | Layout 5   | N/A    | <0.5"    | A               | N/A    |
| DCLK_WR                       | Layout 2   | N/A    | <0.5"=L1 | A+3.5"-L1       | 0.5"   |
| CPUHCLK                       | Layout 3   | <0.1"  | <0.5"    | A+5.2"          | N/A    |
| GMCHHCLK                      |            |        | <0.5"    |                 |        |
| GMCH_3V66                     | Layout 4   | N/A    | <0.5"    | A+8"            | N/A    |
| ICH_3V66                      | Layout 4   | N/A    | <0.5"    | A+8"            | N/A    |
| PCLKICH                       | Layout 4   | N/A    | <0.5"    | A+8"            | N/A    |
| PCLK559A,B; PCLKFWH ; PCLKSIO | Layout 4   | N/A    | <0.5"    | A+8.5" to A+14" | N/A    |
| PCICLKA                       | Layout 1   | N/A    | <0.5"    | A+5" to A+11"   | N/A    |

Note : A < 6"

PCI Bus Routing Requirements

PCI Bus GROUPS

- >> Address/Data Signals: AD[31:0]
- >> Control Signals:
  - C/BE[3:0]#, REQ[4:1]#, GNT[4:1]#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

Hub Interface Routing Requirements

- >> Hub interface data signals shall be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. To break out of the GMCH and the ICH2, the hub interface data signals may be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals shall be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH/ICH2 components.
- >> The maximum trace length for the hub interface data signals is 8 inches. These signals shall each be matched within 0.1 inch of the HLSTB and HLSTB# signals.
- >> HL[10:0] should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. The maximum trace length for the hub interface data signals is 7". These signals shall each be matched within .1" of the HLSTB and HLSTB# signals.

HUB Bus GROUPS

- >> Address/Data Signals: HL[10:0]
- >> Control Signals: HLSTB, HLSTB# (differential strobe pair).

DVO Interface Routing Requirements

- >> Route data signals (LTVDATA[11:0]) with a trace width of 5 mils and a trace spacing of 20 mils. These signals may be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes.
- >> To break out of the GMCH, the DVO data signals may be routed with a trace width of 5 mils and a trace spacing of 5 mils. The signals shall be separated to a trace width of 5 mils and a trace spacing of 20 mils, within 0.3 inch of the GMCH component. The maximum trace length for the DVO data signals is 7 inches. These signals shall each be matched within 0.1 inch of the LTVCLKOUT[1] and LTVCLKOUT[0] signals.
- >> Route the LTVCLKOUT[1:0] signals 5 mils wide and 20 mils apart. This signal pair shall be a minimum of 20 mils from any adjacent signals. The maximum length for LTVCLKOUT[1:0] is 7 inches and the two signals shall be the same length.

AC97 Interface Routing Requirements

- >> To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

- >> Special consideration must be given for the ground return paths for the analog signals.

- >> Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals shall be located as far as possible from each other.

- >> Partition the board with all analog components grouped together in one area and all digital components in another.

- >> Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.

- >> Keep digital signal traces, especially the clocks, as far as possible from the analog input and voltage reference pins.

- >> Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.

- >> Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which could cause a ground loop, thereby greatly increasing EMI issues and degrading the analog and digital signal quality.

- >> Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

- >> All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.

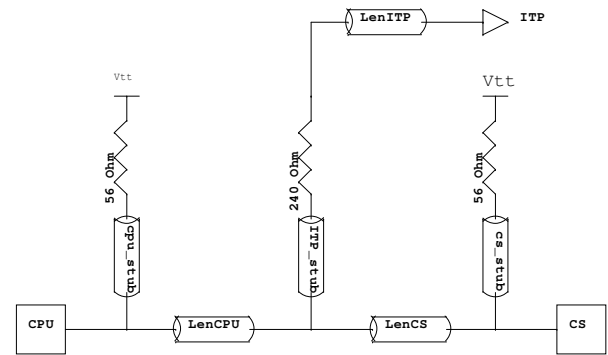
- >> Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

- >> Locate the crystal or oscillator close to the codec.

Power Supply Routing Requirements

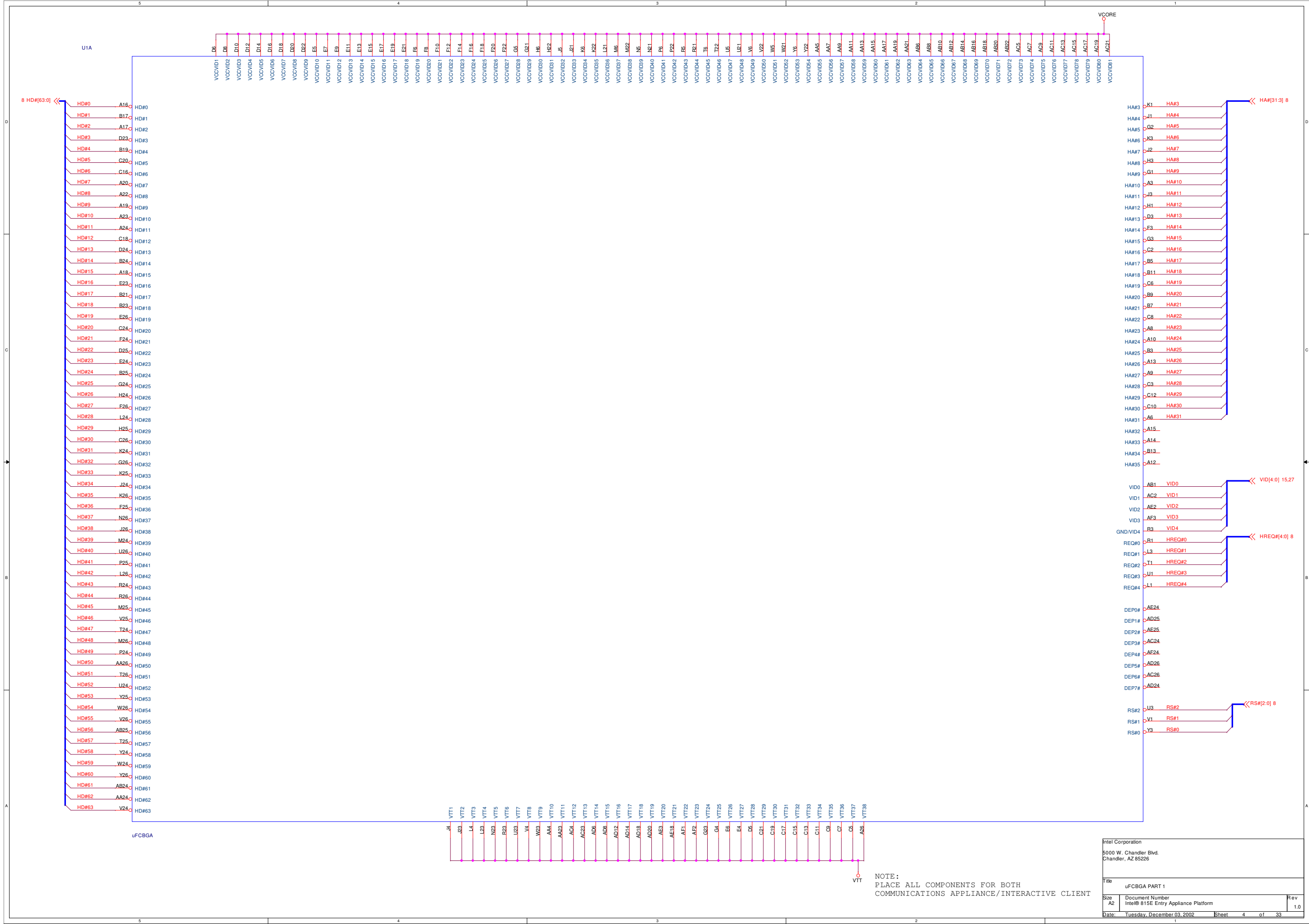
- >> All unrelated signals and power planes shall be kept away from the switching circuits, devices, magnetics, and traces.
- >> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.
- >> Refer to the power supply data sheets and the schematic sheets for more detail.

RESET#/RESET2# Routing Requirements



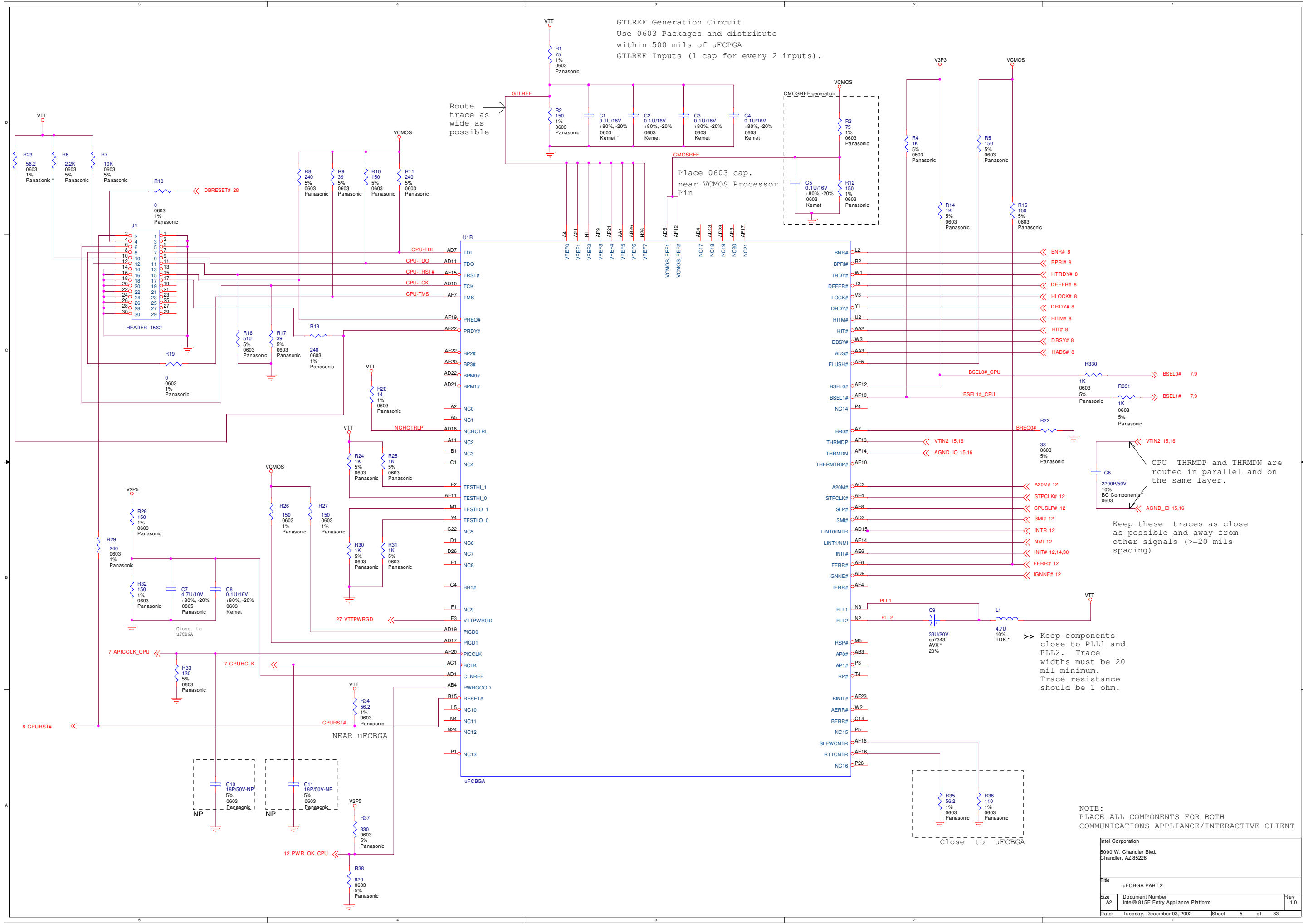
Routing Solution :

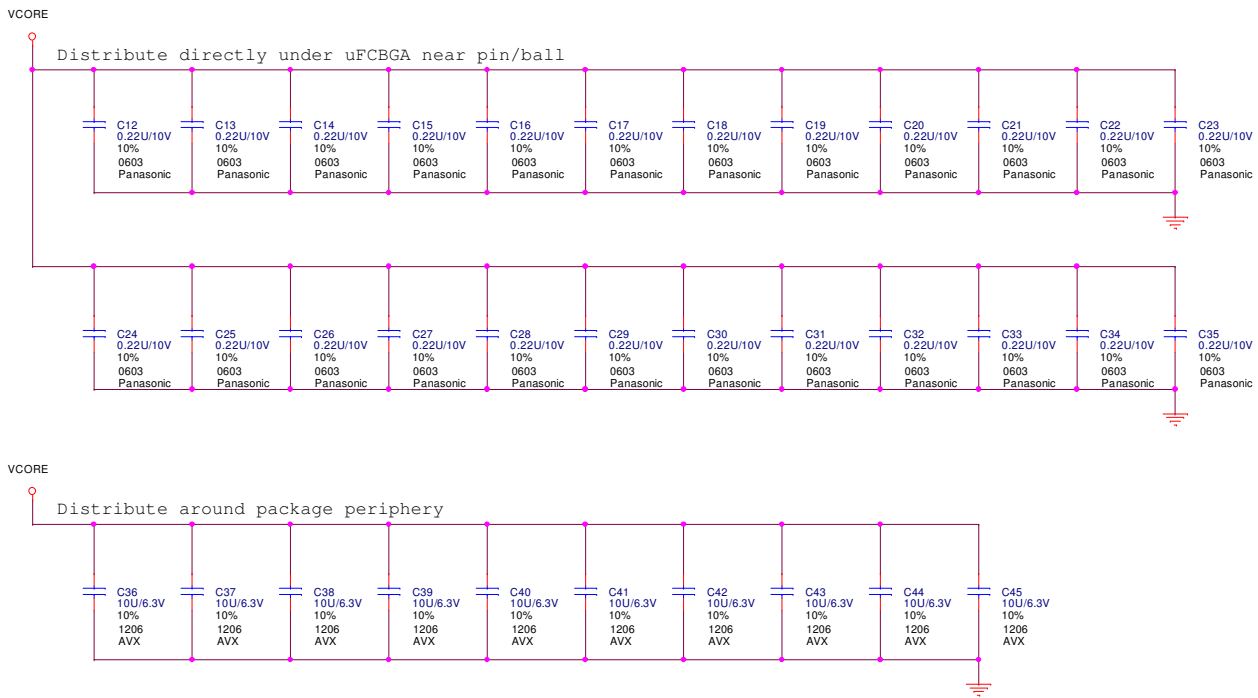
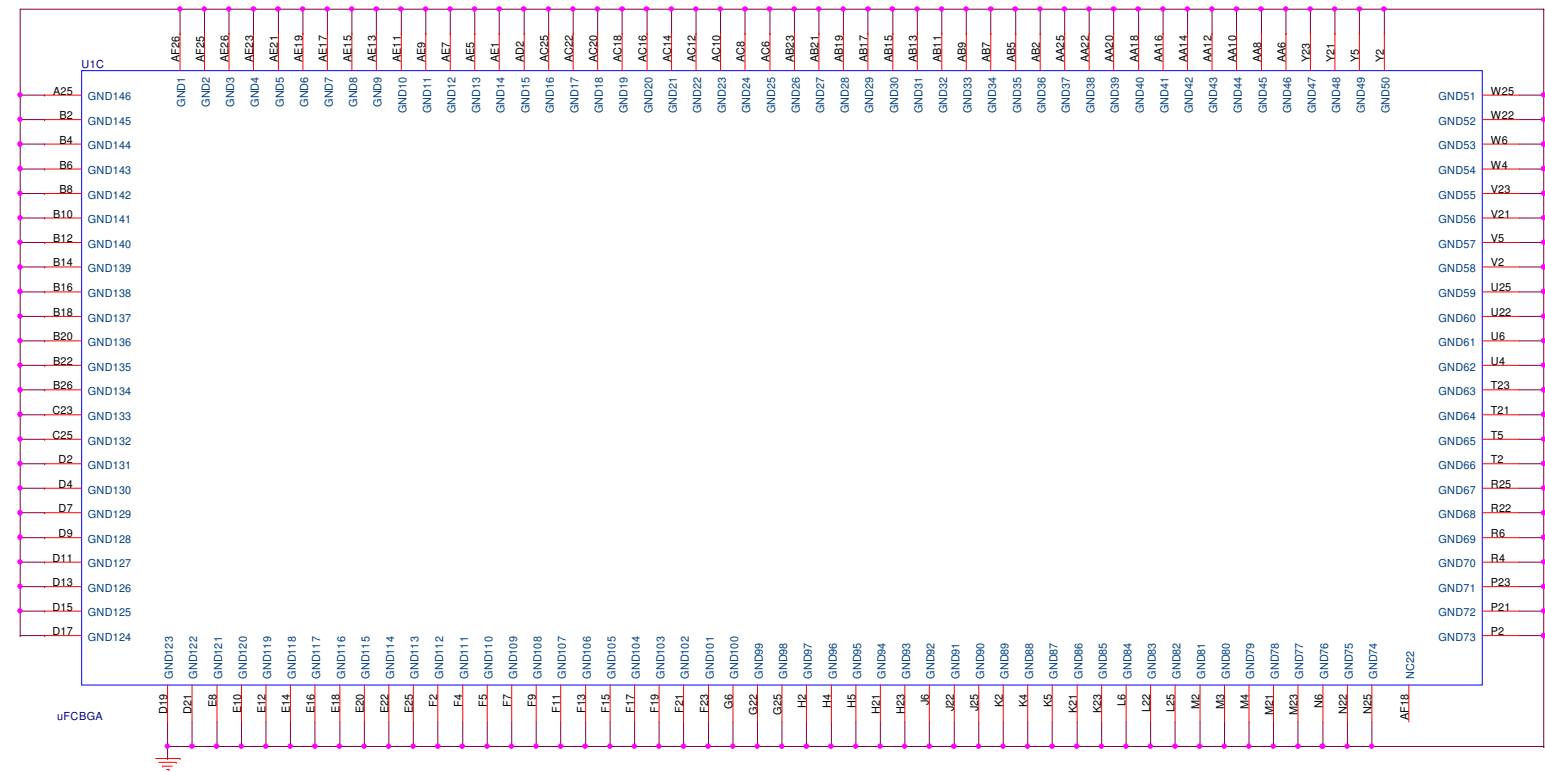
| Parameter | Minimum (in)      | Maximum (in) |
|-----------|-------------------|--------------|
| LenCS     | 0.5               | 1.5          |
| LenITP    | 1                 | 3            |
| LenCPU    | 0.5               | 1.5          |
| cs stub   | 0.5               | 1            |
| cpu stub  | 0.5               | 1            |
| ITP stub  | short as possible |              |



NOTE:  
PLACE ALL COMPONENTS FOR BOTH  
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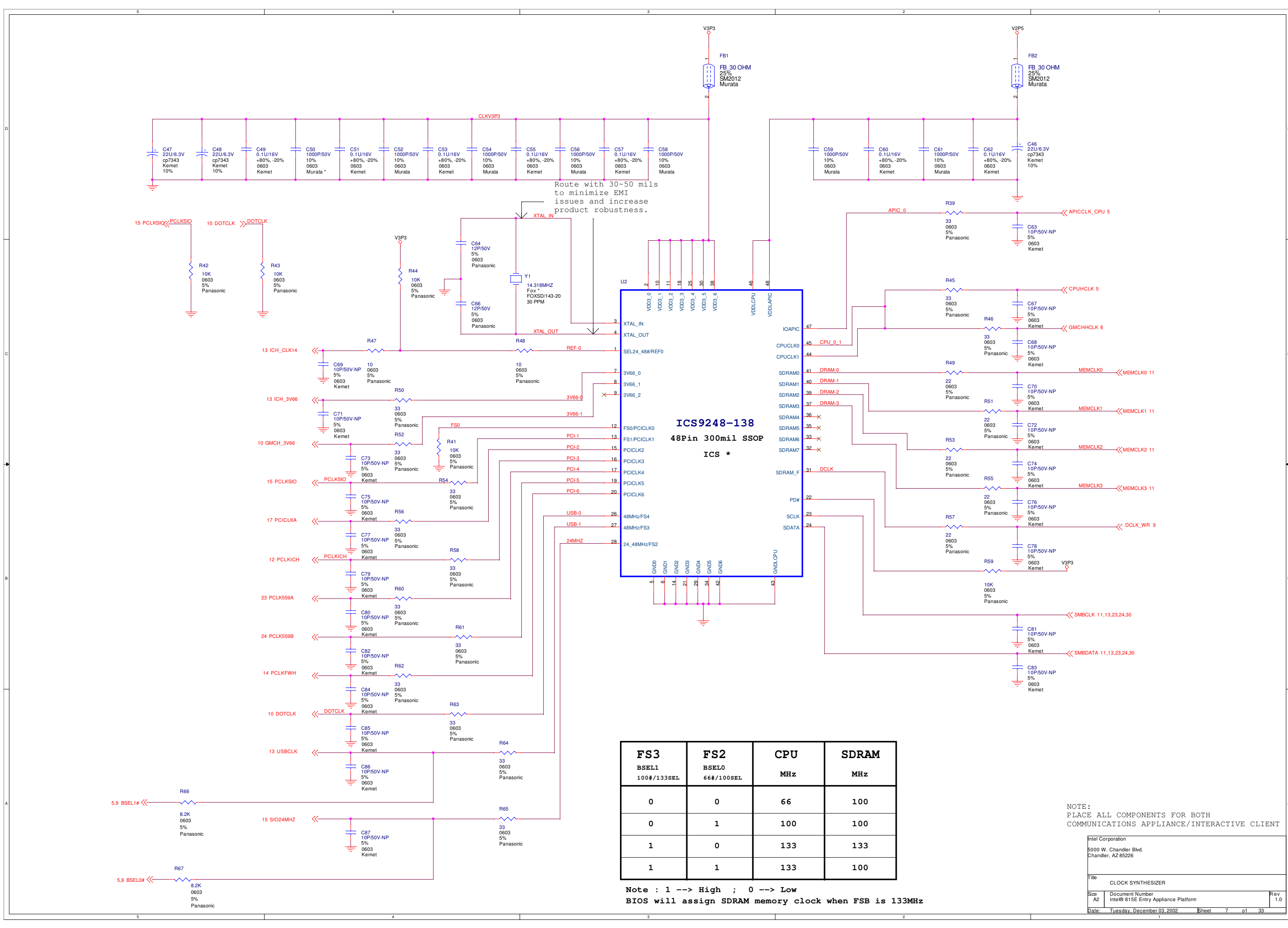
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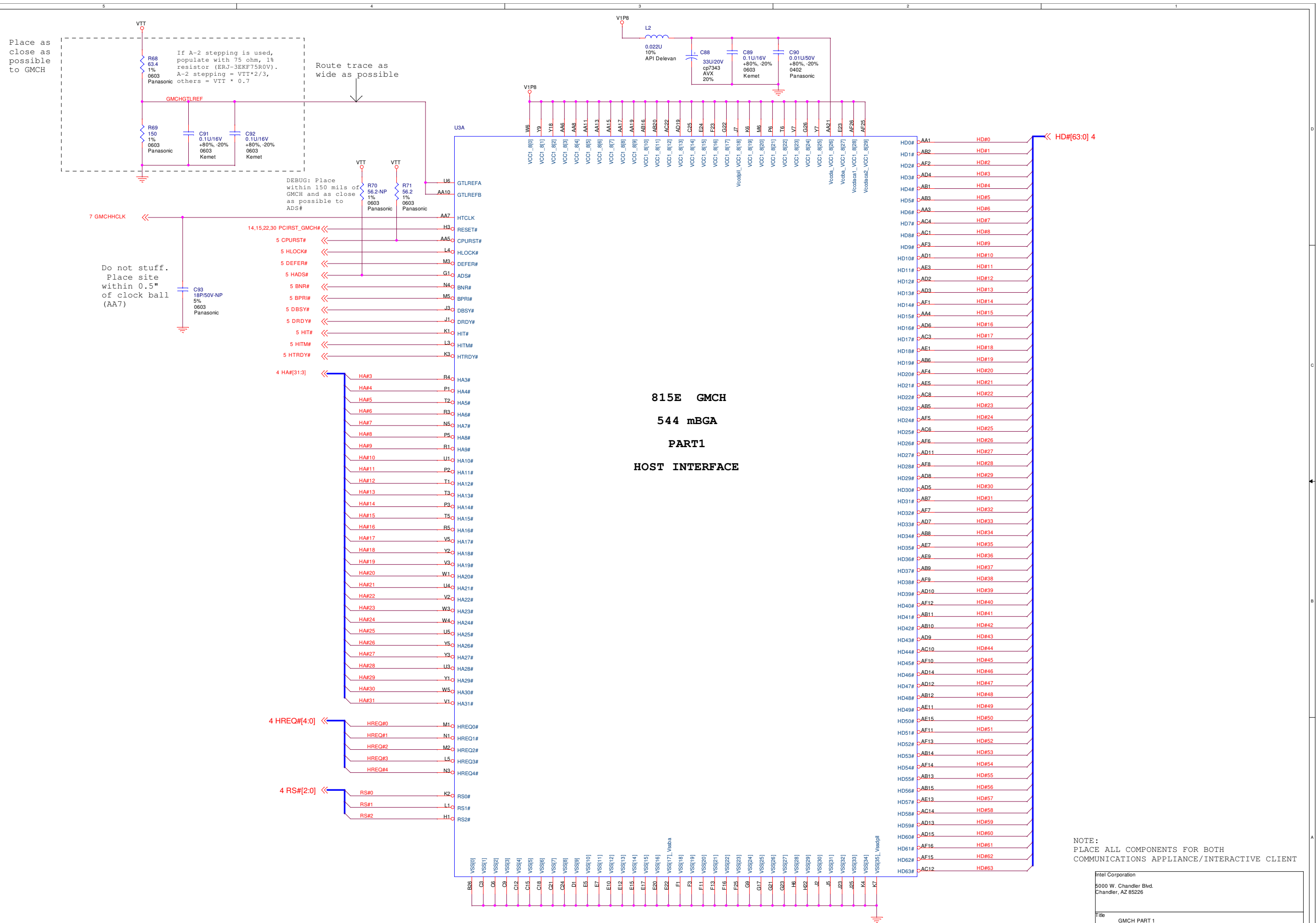


| FS3<br>BSEL1<br>100#/133SEL | FS2<br>BSEL0<br>66#/100SEL | CPU<br>MHz | SDRAM<br>MHz |
|-----------------------------|----------------------------|------------|--------------|
| 0                           | 0                          | 66         | 100          |
| 0                           | 1                          | 100        | 100          |
| 1                           | 0                          | 133        | 133          |
| 1                           | 1                          | 133        | 100          |

Note : 1 --> High ; 0 --> Low  
BIOS will assign SDRAM memory clock when FSB is 133MHz

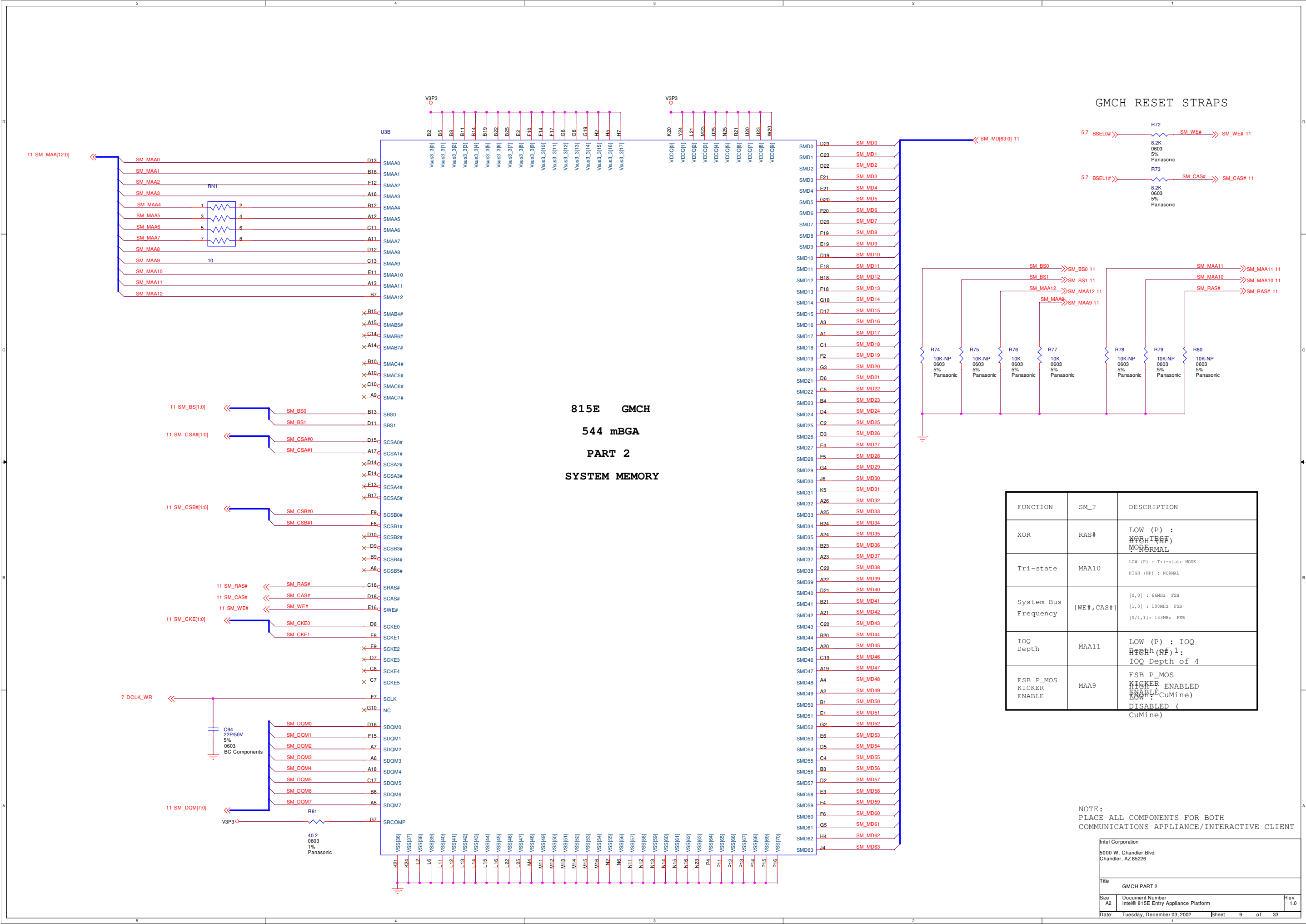
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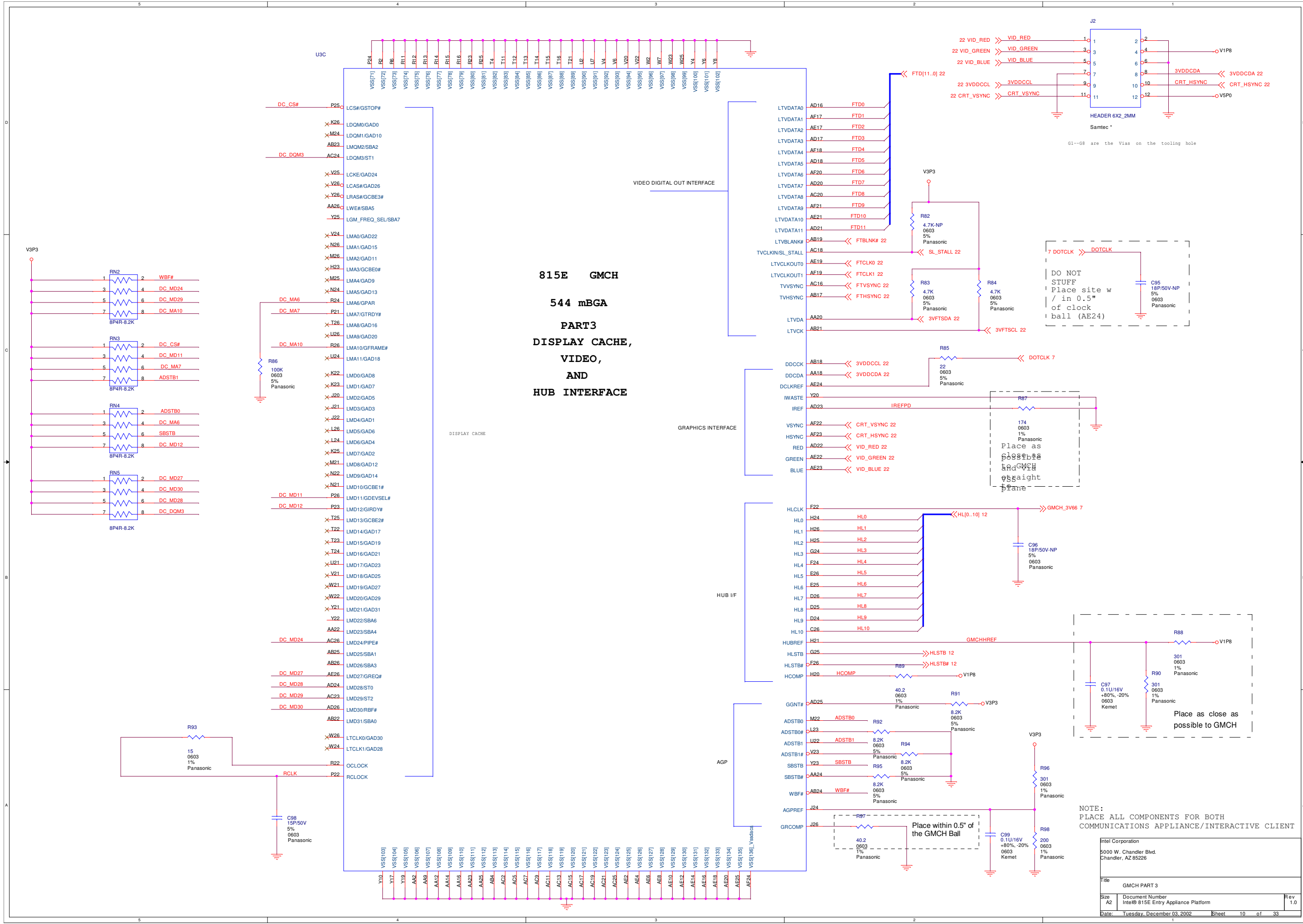
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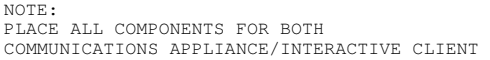


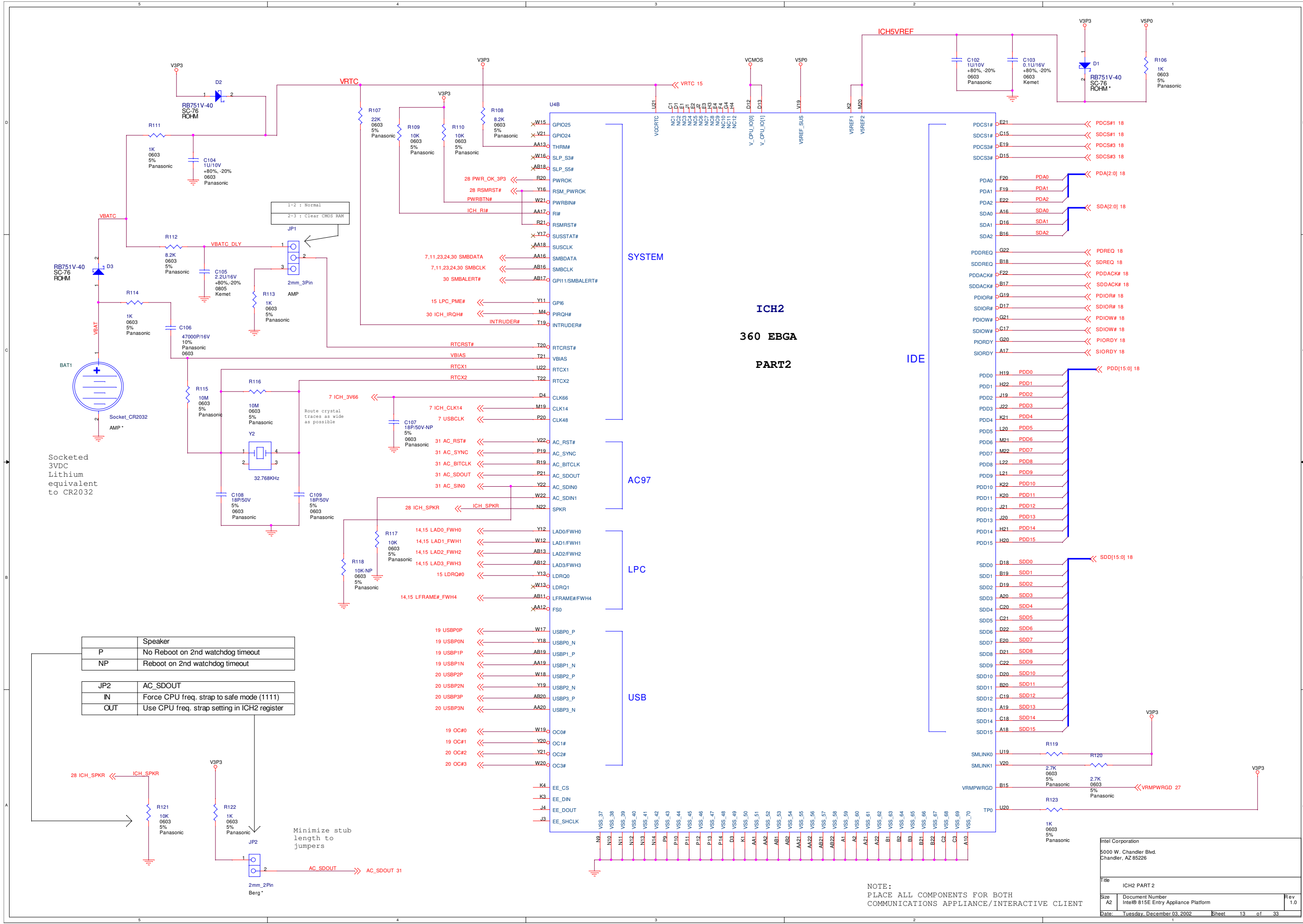




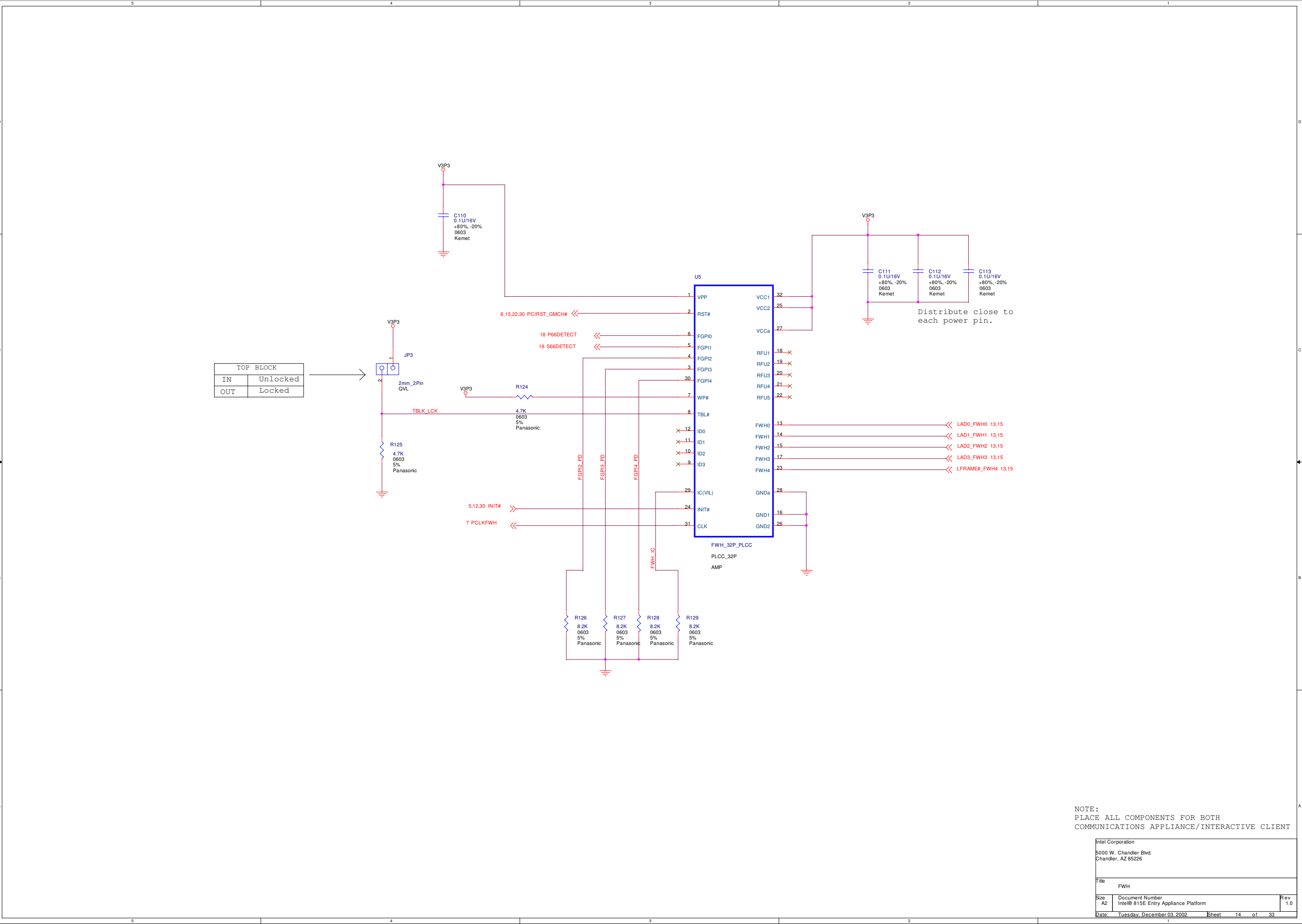


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| Date: | Tuesday, December 03, 2002           |  |  | Sheet | 11 |  | of 33 |



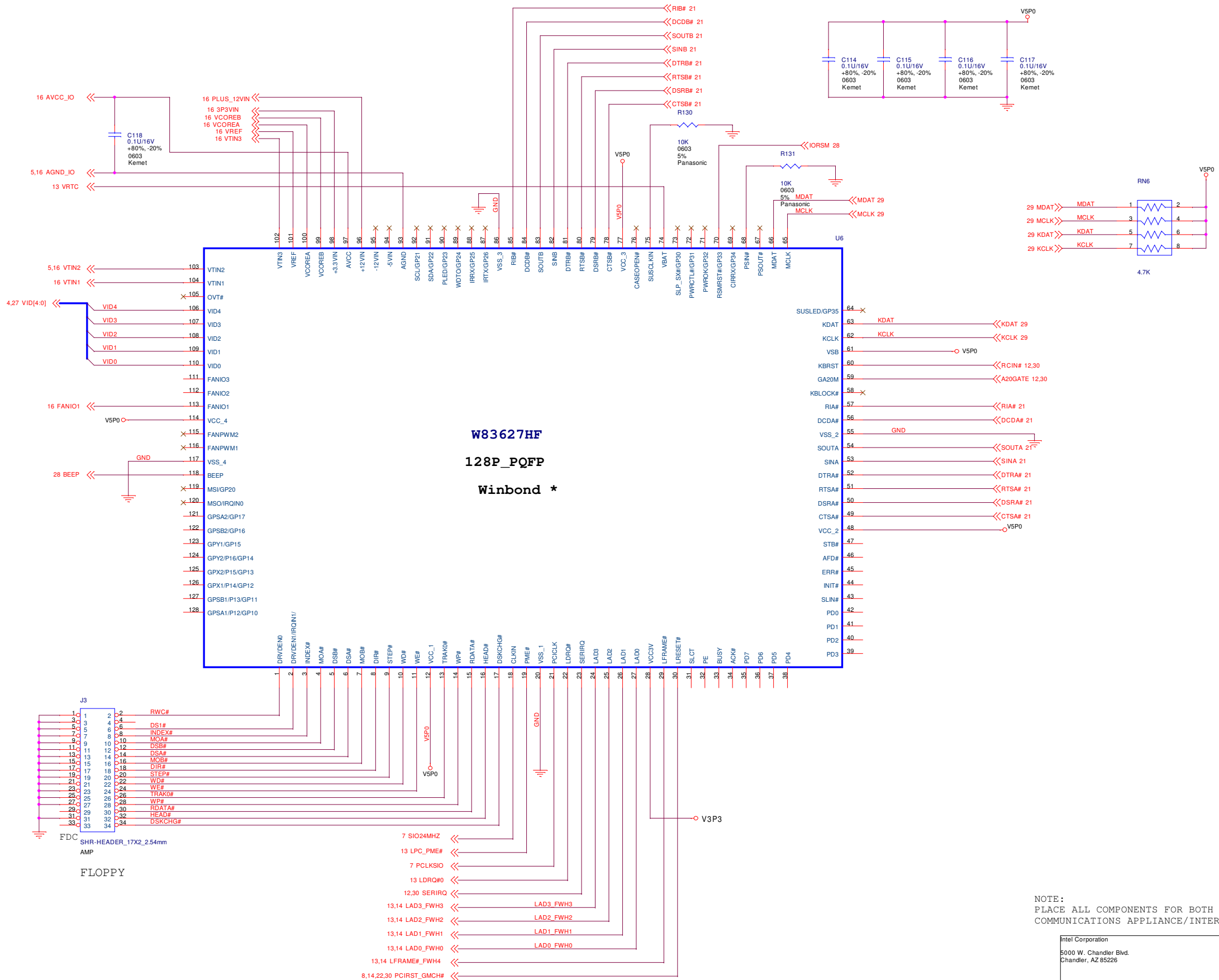


NOTE:  
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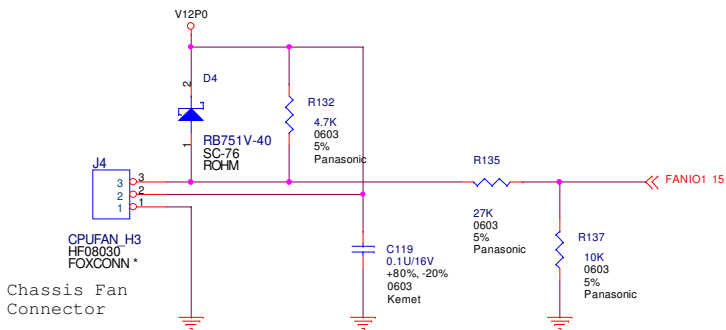
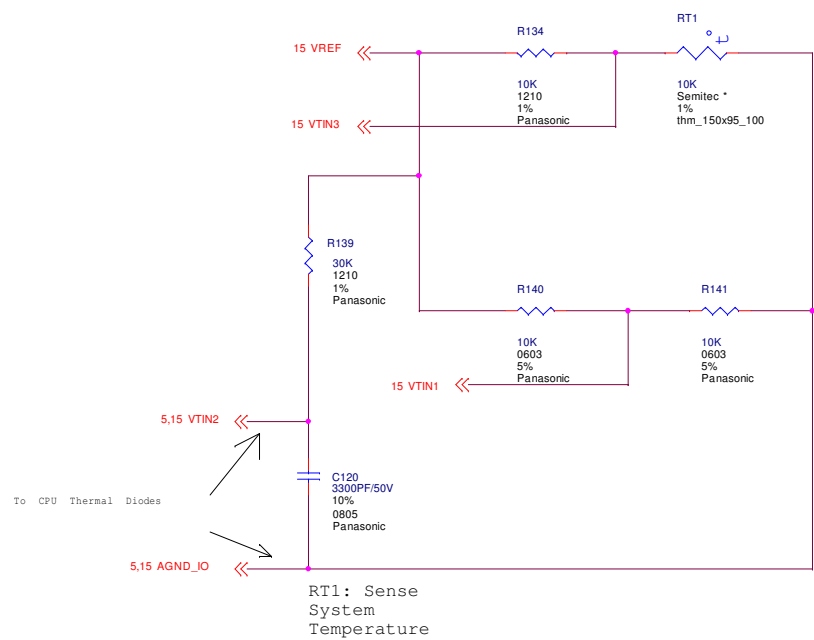
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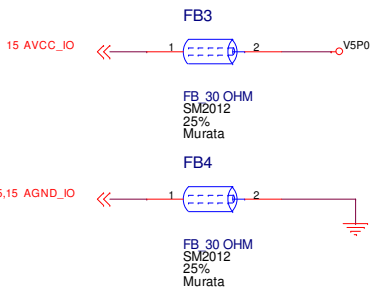
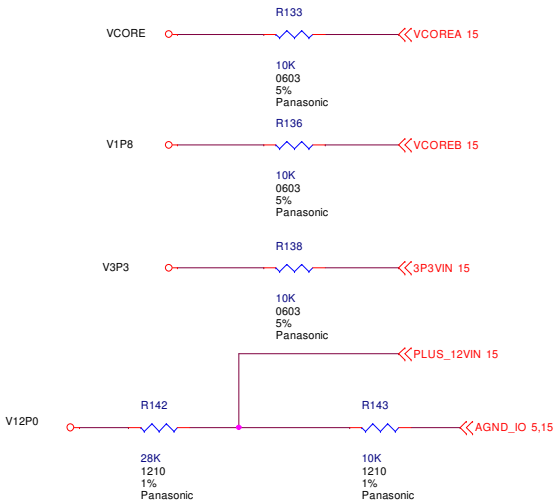
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Temperature Sensing



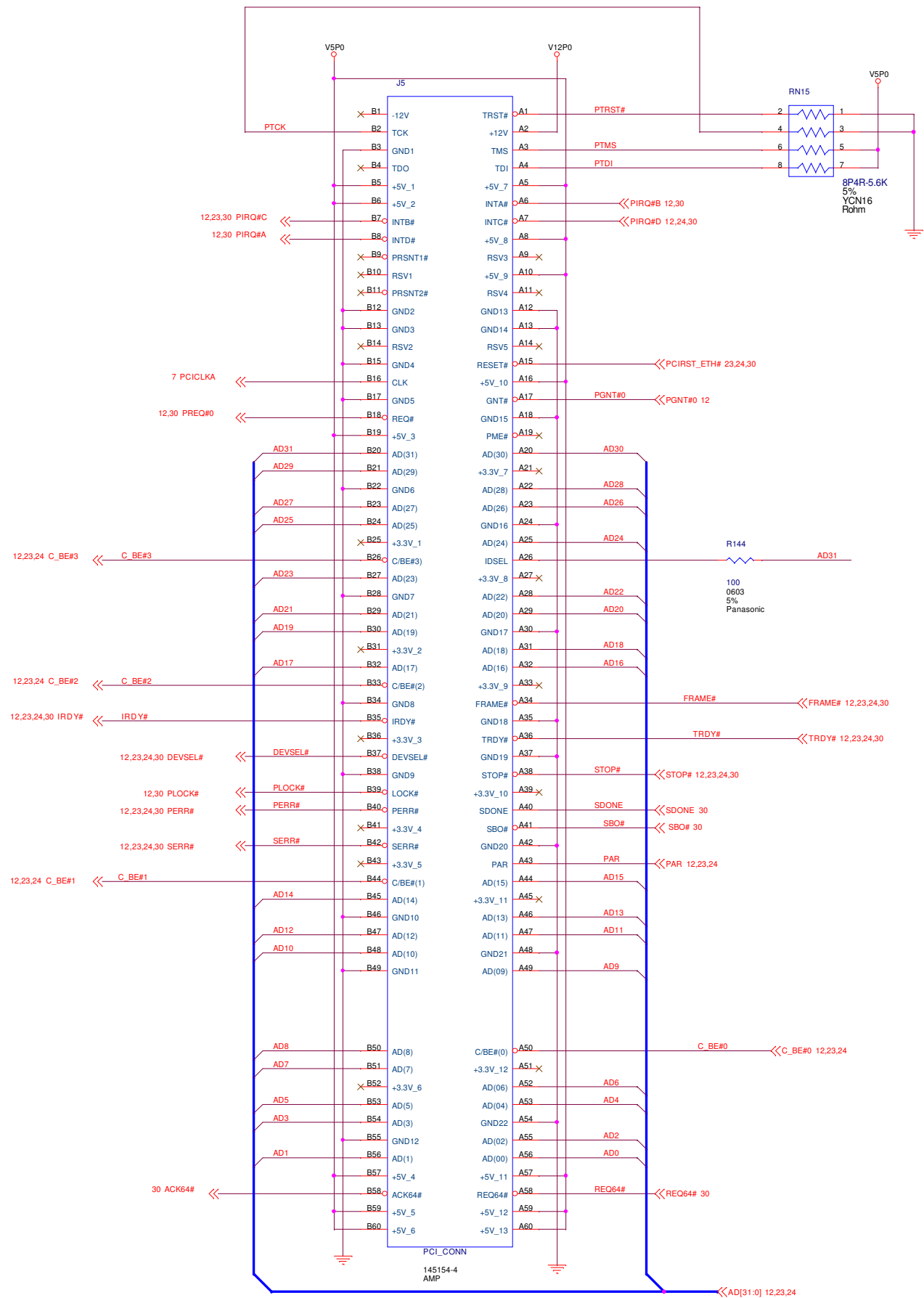
Voltage Sensing



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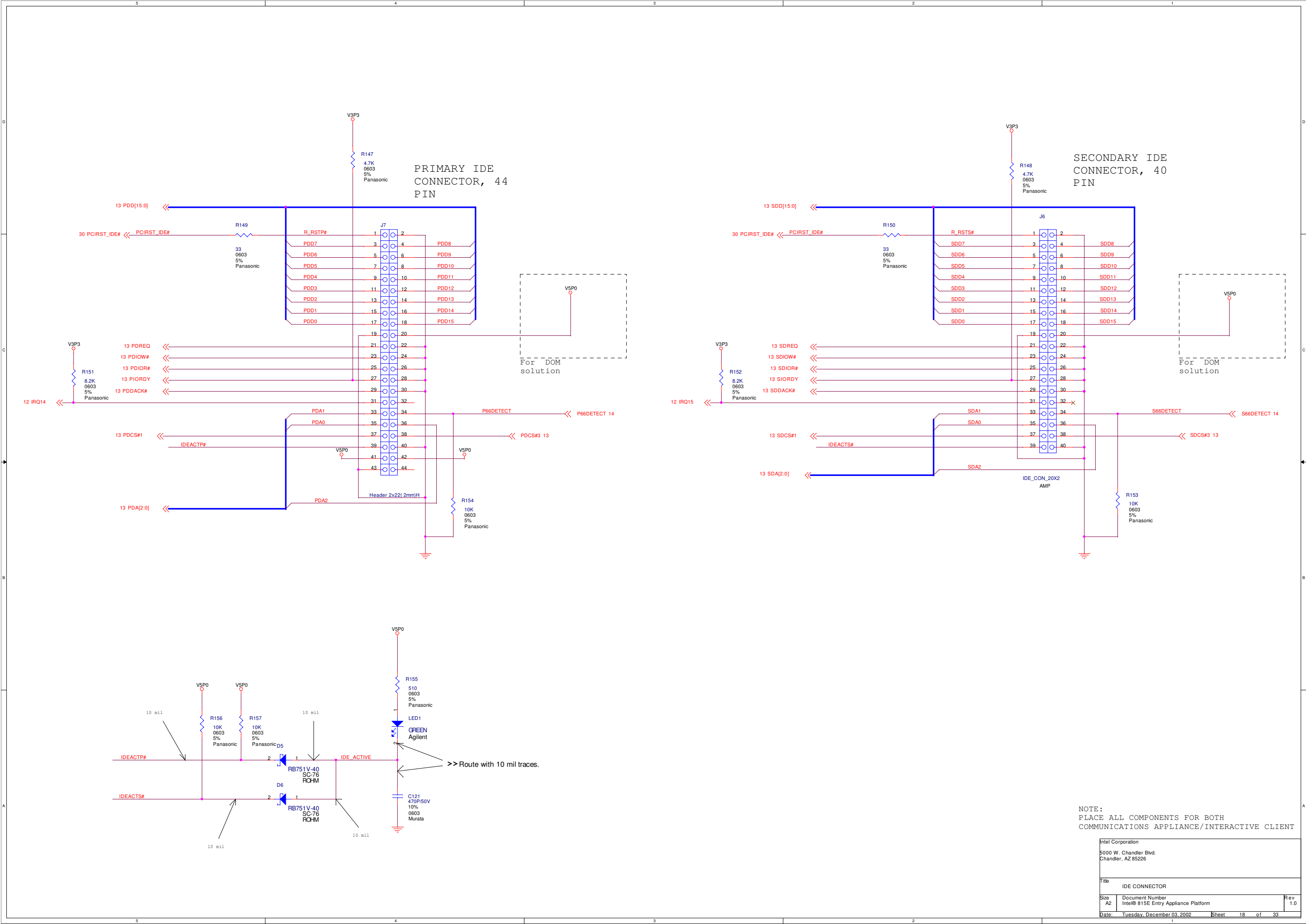


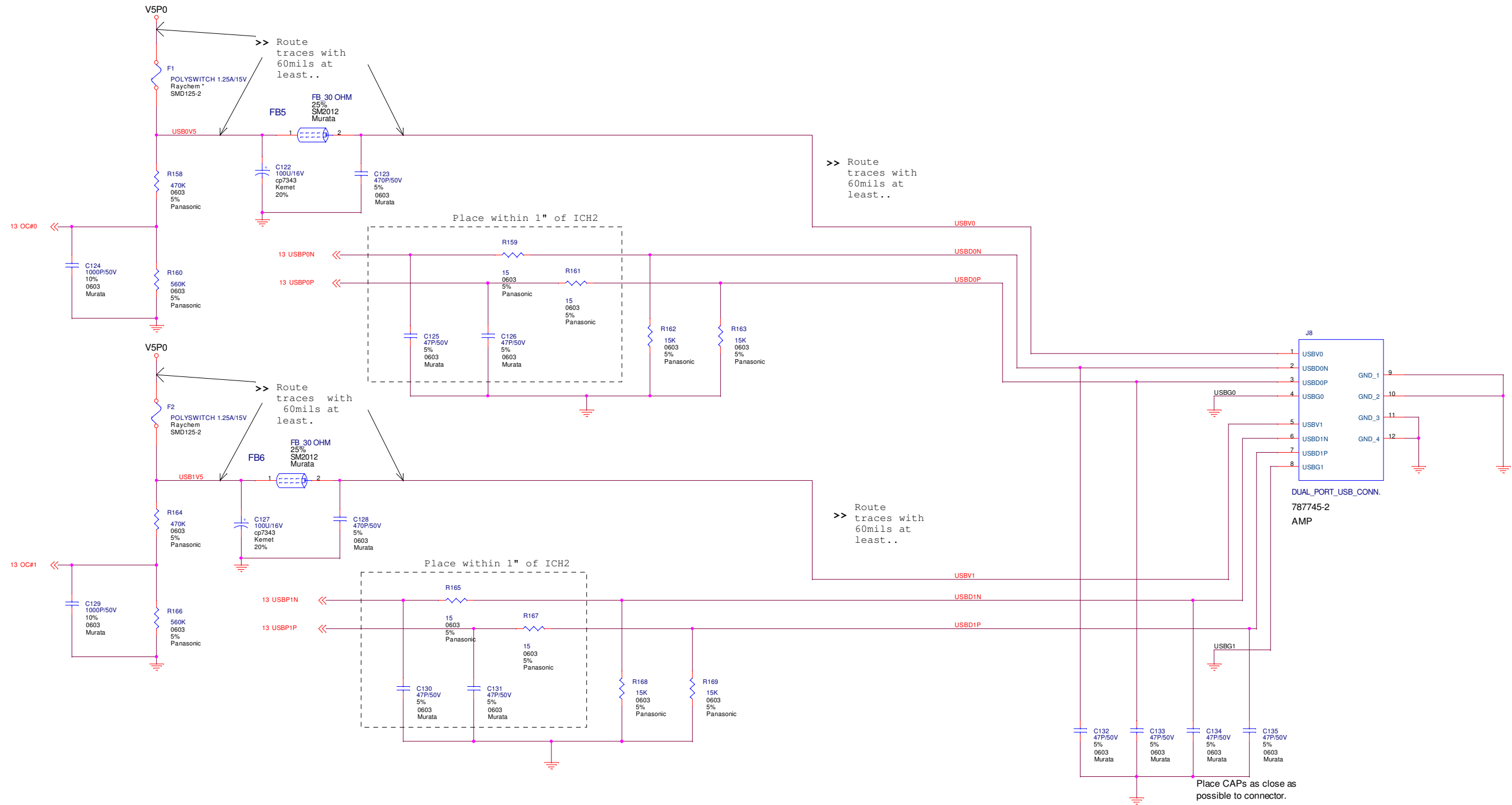


5V PCI CONN., NO 3.3V AND -12V SUPPORT  
IDSEL=AD31

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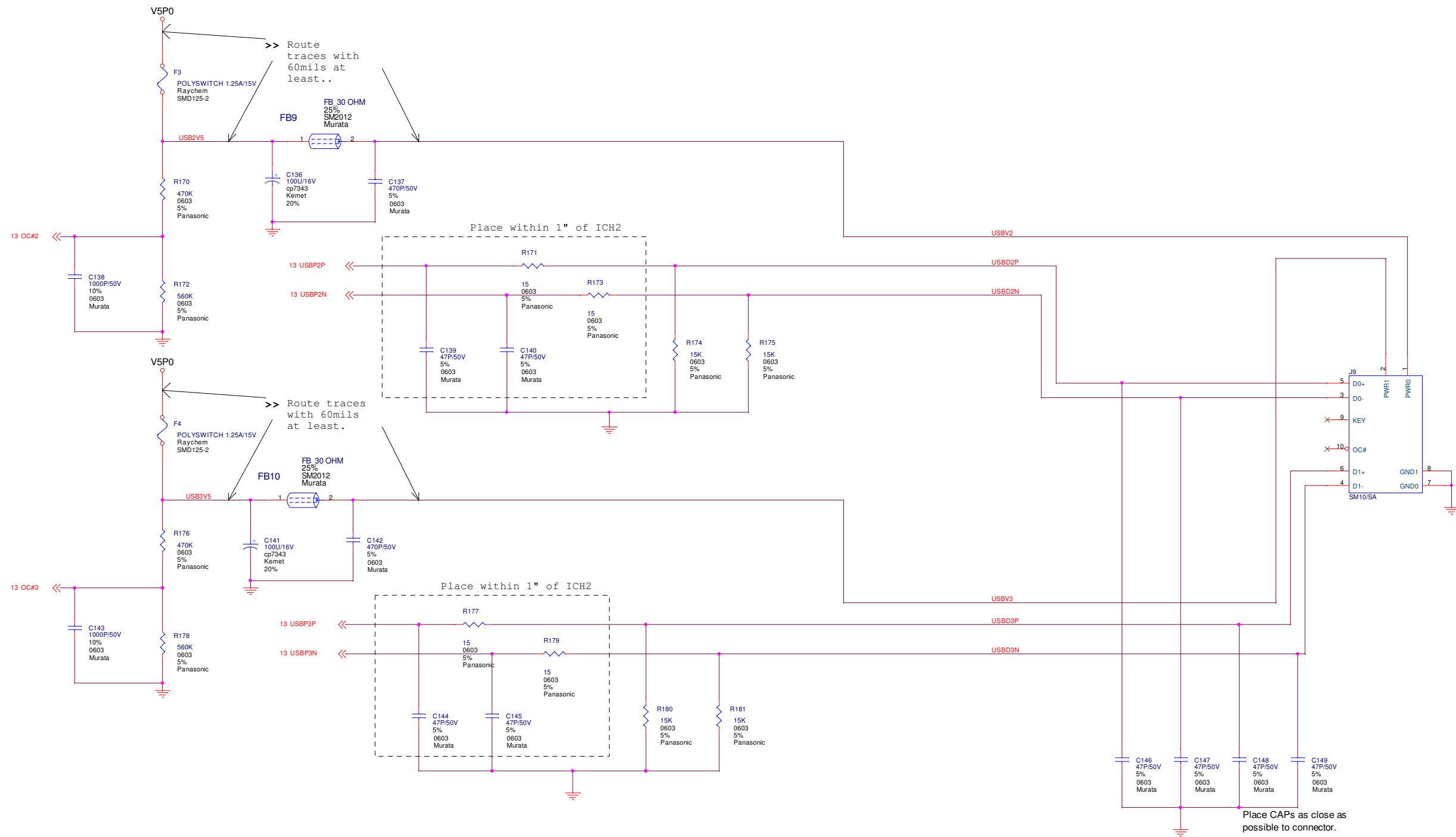
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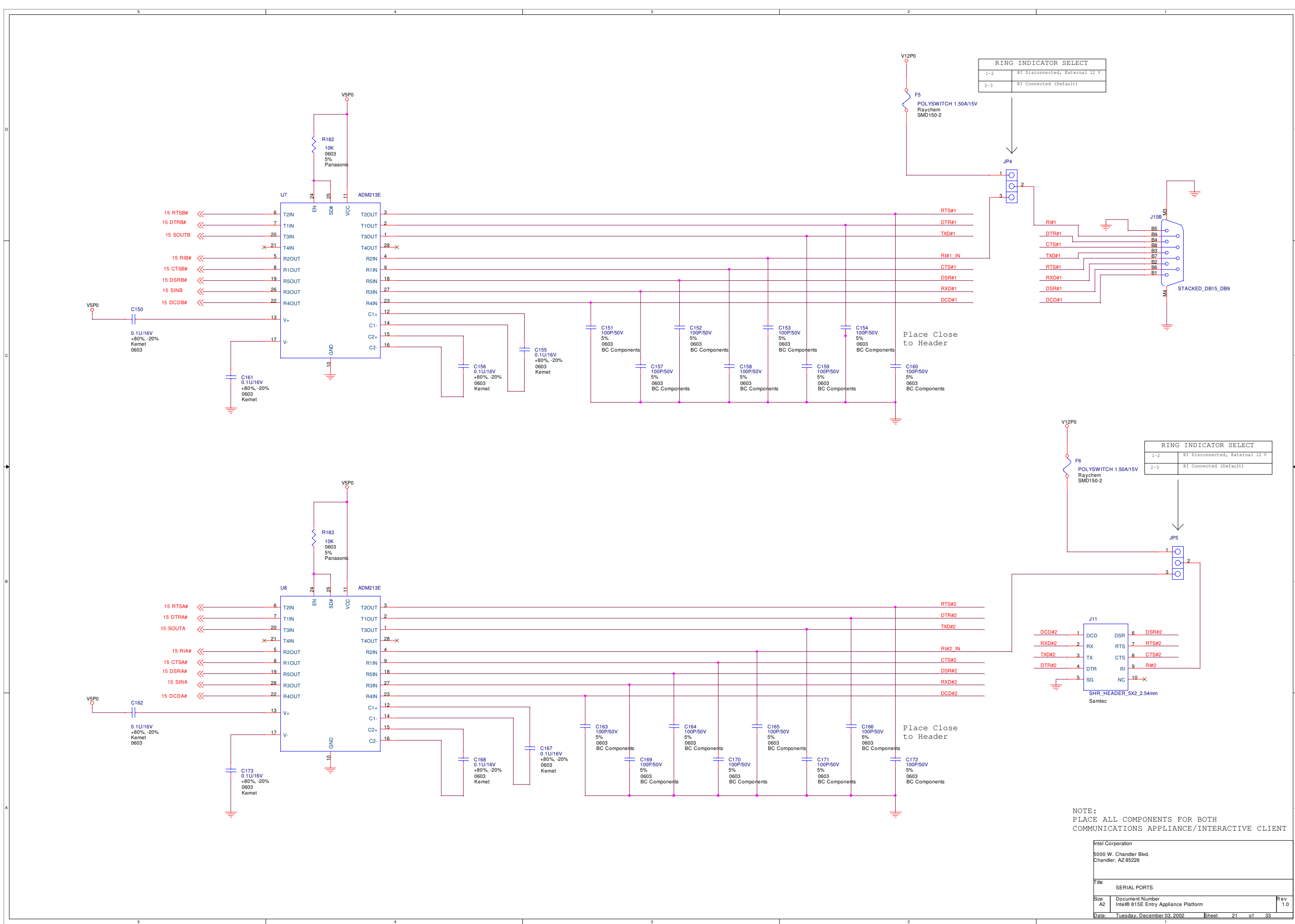
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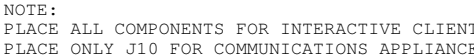
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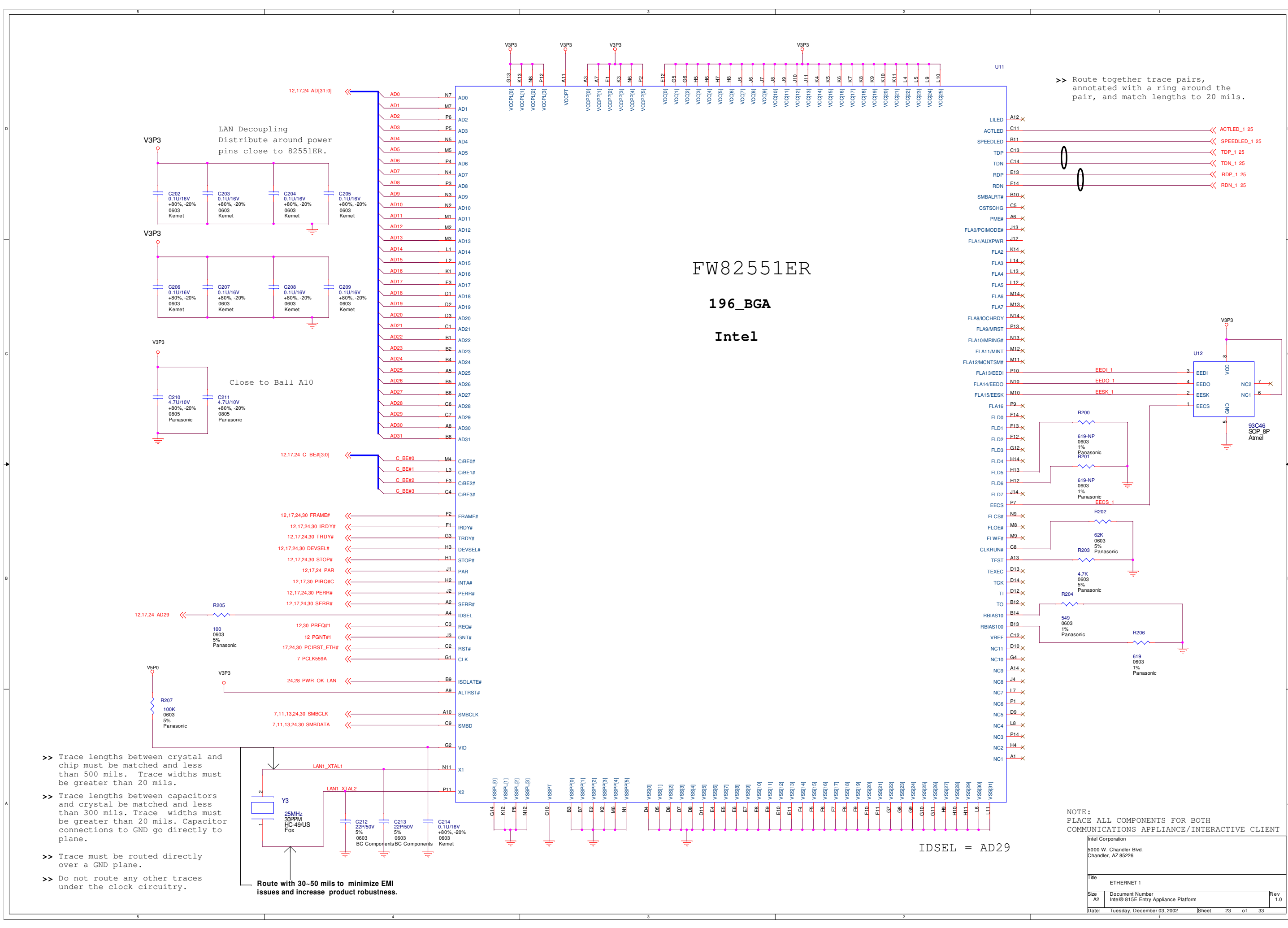
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>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.

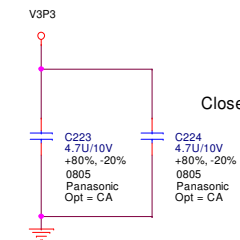
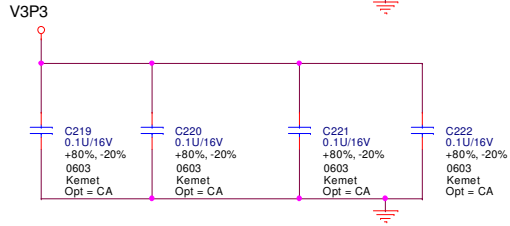
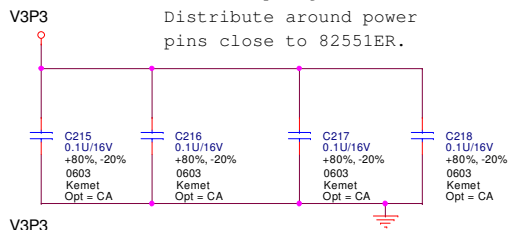
FW82551ER  
196\_BGA  
Intel

NOTE:  
PLACE ALL COMPONENTS FOR BOTH  
COMMUNICATIONS APPLIANCE/INTERACTIVE CLIENT

|   |   |            |
|---|---|------------|
| Intel Corporation<br>5000 W. Chandler Blvd.<br>Chandler, AZ 85226 |   |            |
| Title<br>ETHERNET 1   |   |            |
| Size<br>A2  | Document Number<br>Intel® 815E Entry Appliance Platform | Rev<br>1.0 |
| Date: Tuesday, December 03, 2002 Sheet 23 of 33                   |   |            |

IDSEL = AD29

LAN Decoupling  
Distribute around power  
pins close to 82551ER.



Close to Ball A10

12,17,23 C\_BE#(3:0)

12,17,23,30 FRAME#

12,17,23,30 IRDY#

12,17,23,30 TRDY#

12,17,23,30 DEVSEL#

12,17,23,30 STOP#

12,17,23 PAR

12,17,30 PIQ#

12,17,23,30 PERR#

12,17,23,30 SERR#

12,30 PREQ#2

12 PGNT#2

17,23,30 PCIRST\_ETH#

7 PCLK559B

23,28 PWR\_OK\_LAN

7,11,13,23,30 SMBCLK

7,11,13,23,30 SMBDATA

LAN2\_XTAL1

LAN2\_XTAL2

25MHz 30PPM HC-49US Fox Opt = CA

C225 22p/50V 5% 0603 BC Components Opt = CA

C226 22p/50V 5% 0603 BC Components Opt = CA

C227 0.1u/16V +80%, -20% 0603 Kemet Opt = CA

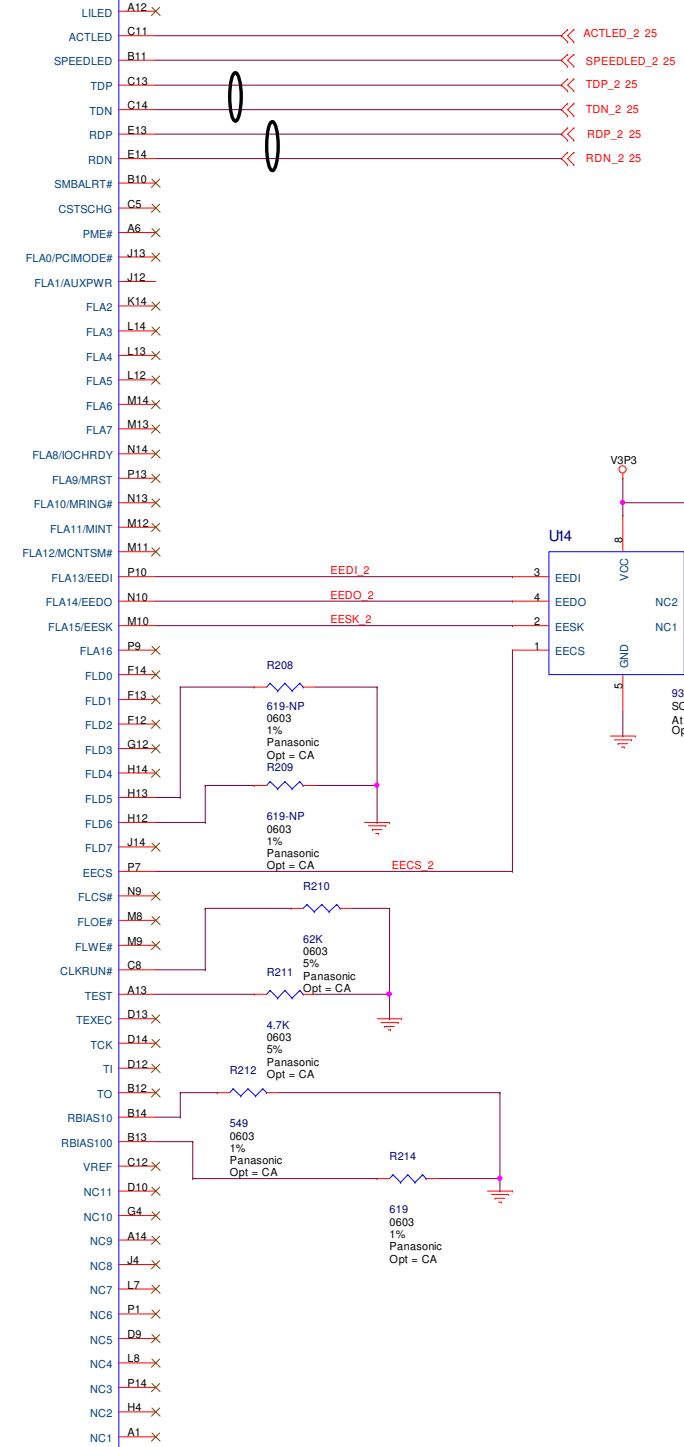
Route with 30-50 mils to minimize EMI  
issues and increase product robustness.

FW82551ER

196\_BGA

Intel

>> Route together trace pairs,  
annotated with a ring around the  
pair, and match lengths to 20 mils.



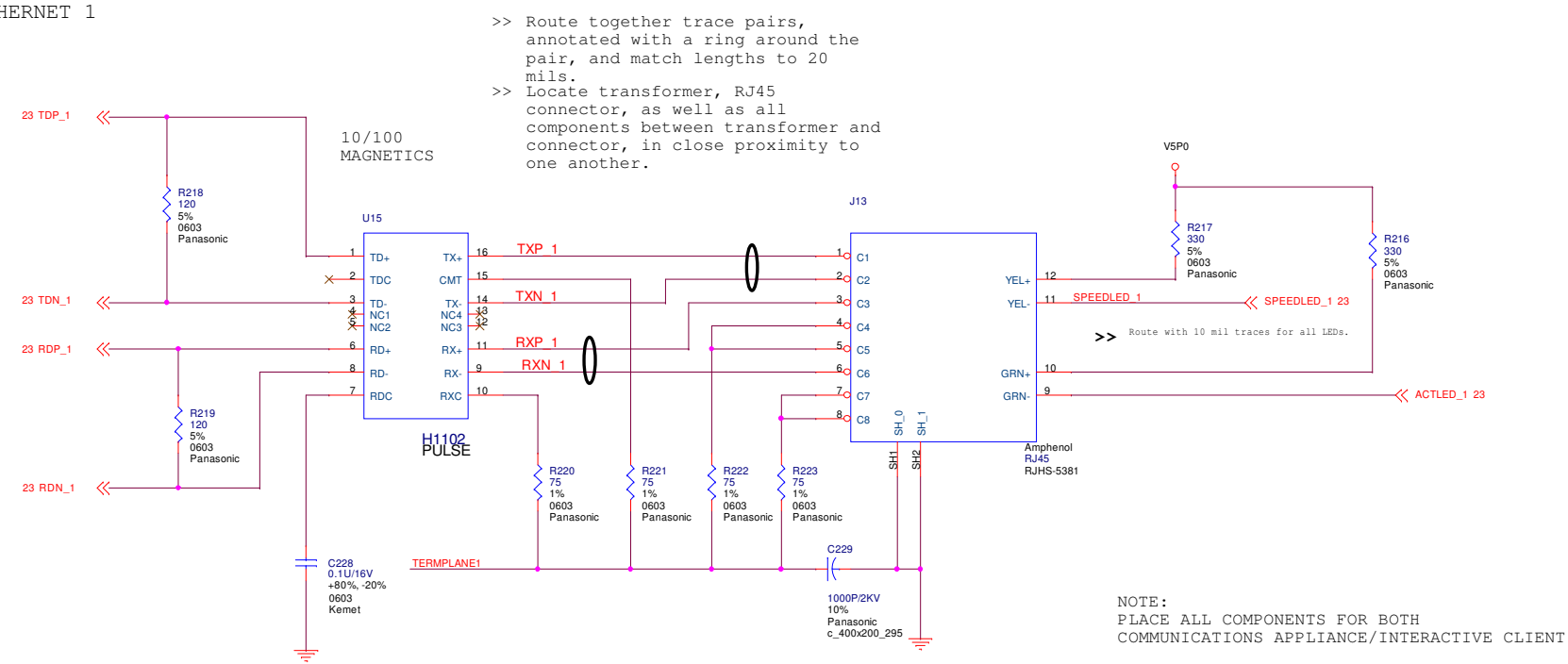
NOTE:  
NO COMPONENTS PLACED FOR INTERACTIVE CLIENT  
PLACE ALL COMPONENTS FOR COMMUNICATIONS APPLIANCE

|   |   |            |
|---|---|------------|
| Intel Corporation<br>5000 W. Chandler Blvd.<br>Chandler, AZ 85226 |   |            |
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| Size<br>A2  | Document Number<br>Intel® 815E Entry Appliance Platform | Rev<br>1.0 |
| Date:<br>Tuesday, December 03, 2002                               | Sheet<br>24   | of<br>33   |

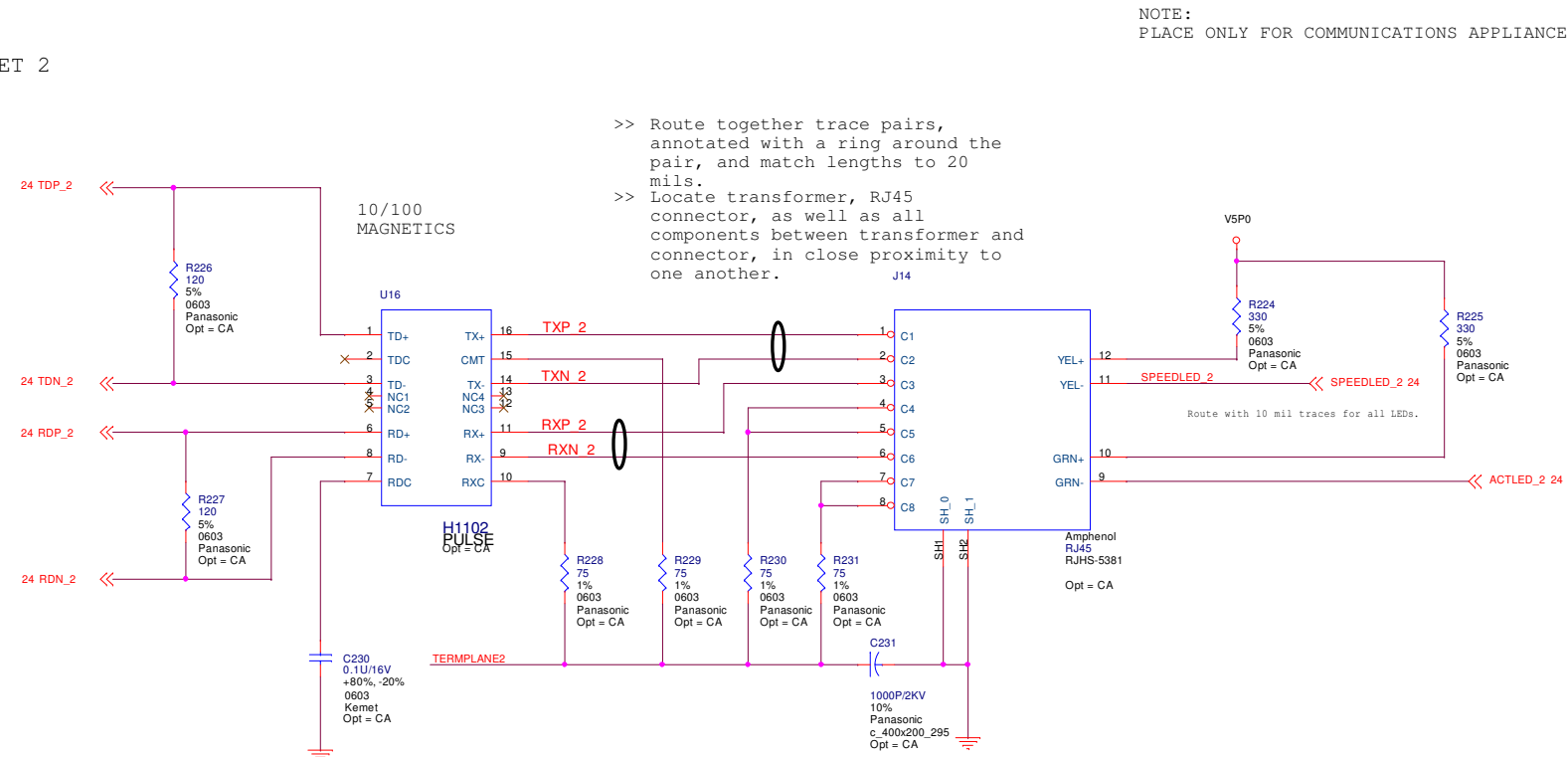
IDSEL = AD30



ETHERNET 1



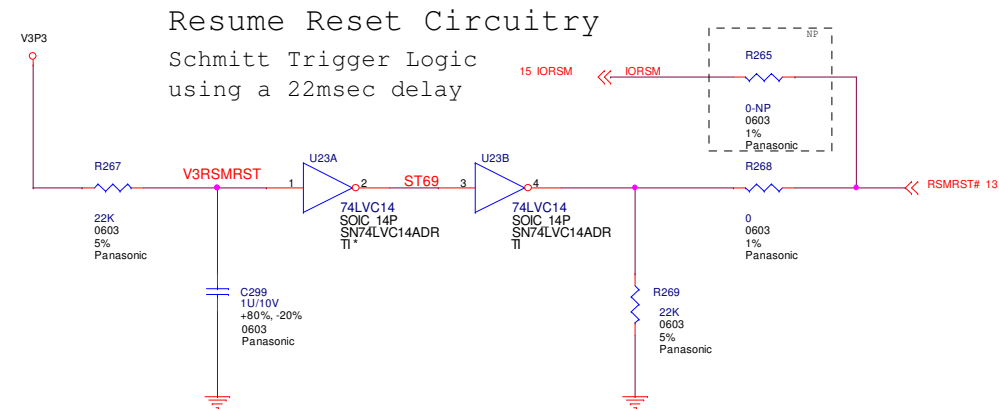
ETHERNET 2



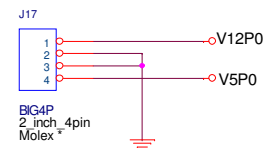
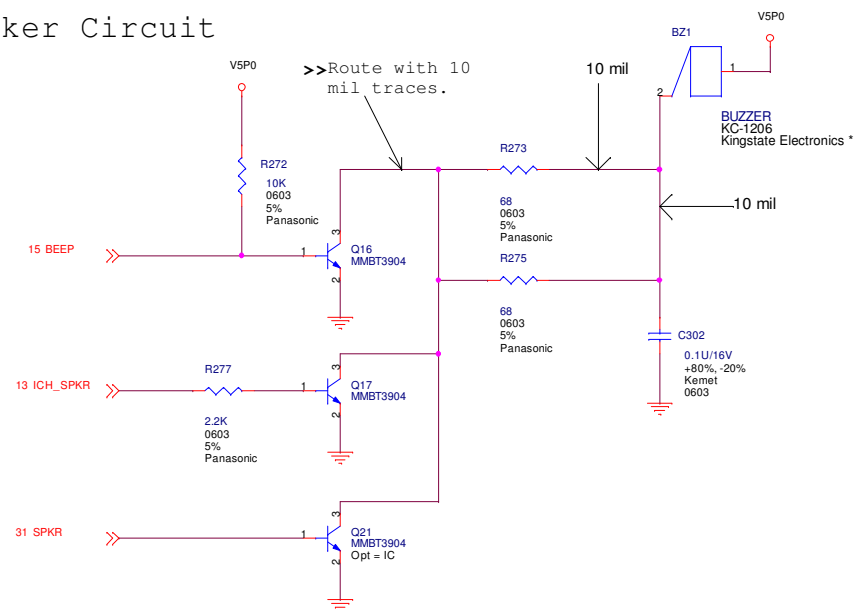




## Power Connector and Reset Control

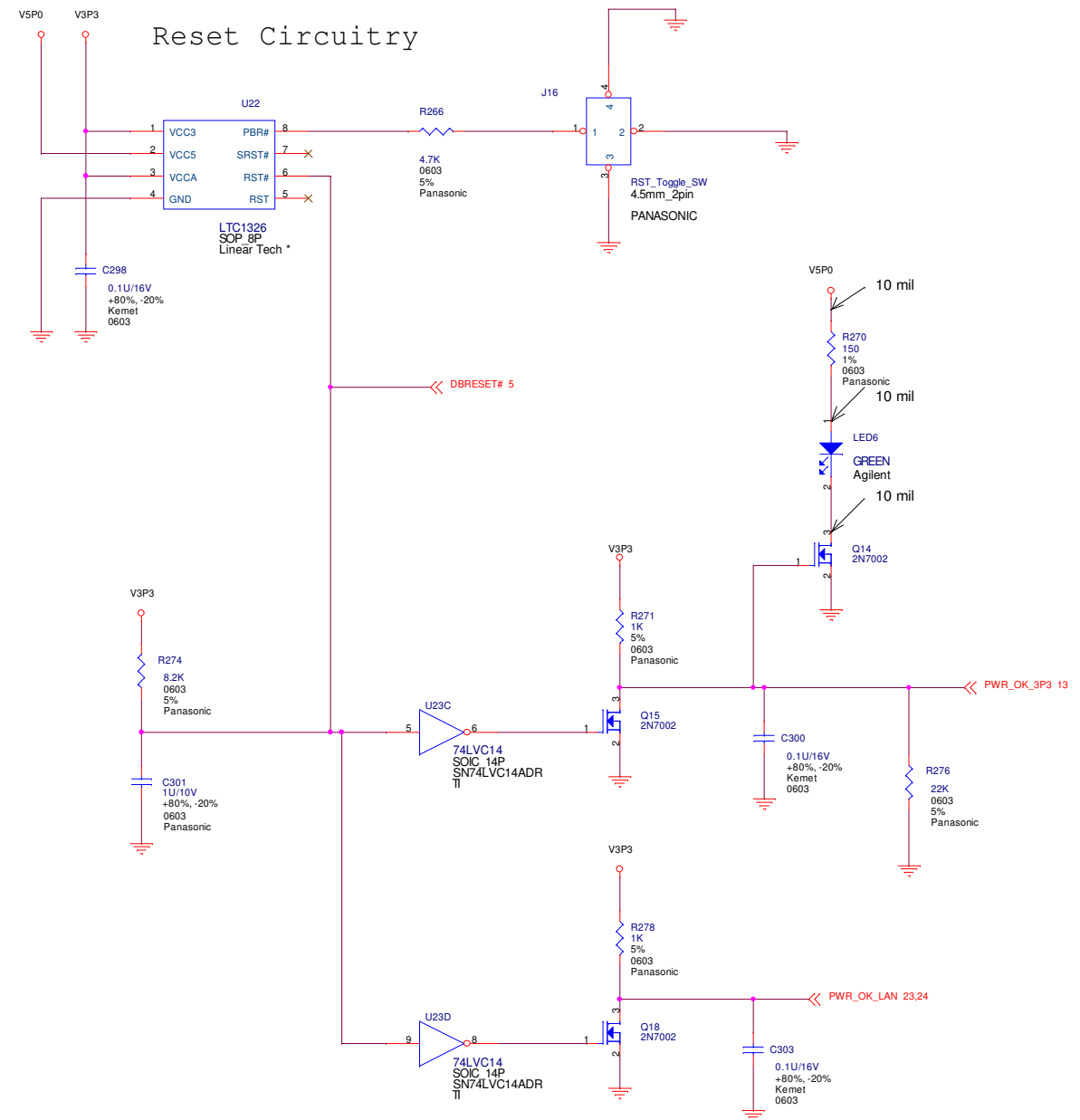


## Speaker Circuit



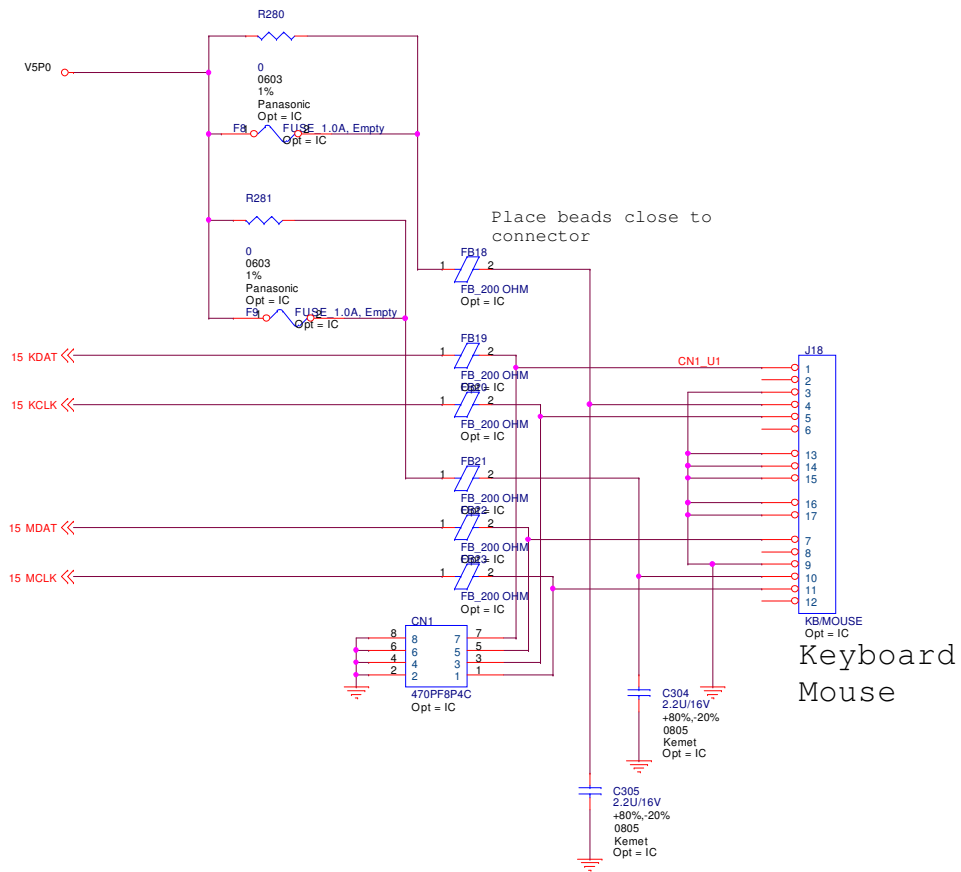
FOR HDD POWER

## Reset Circuitry



NOTE:  
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT  
PLACE ALL BUT Q21 FOR COMMUNICATIONS APPLIANCE

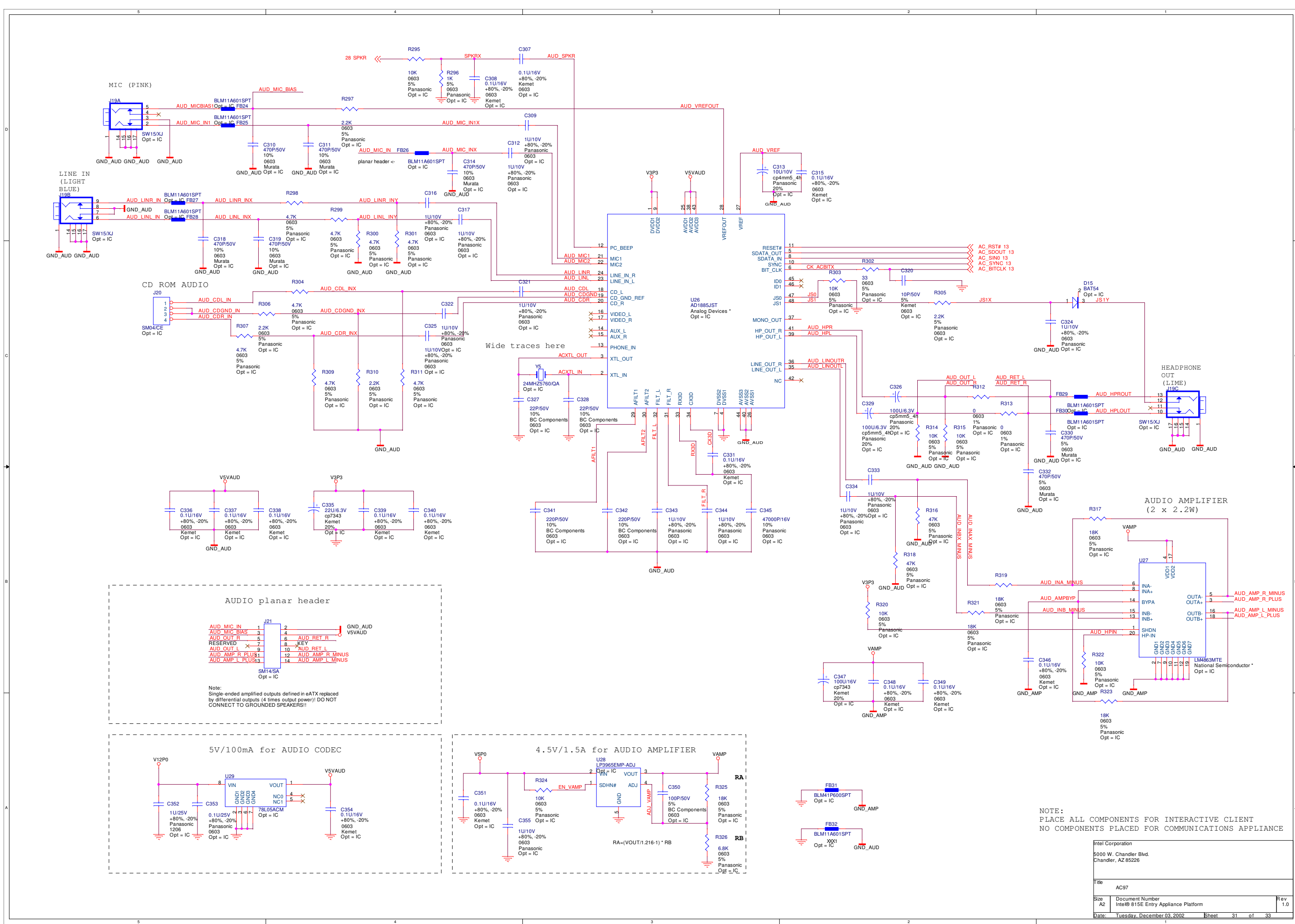
|                        |   |            |          |
|------------------------|---|------------|----------|
| Intel Corporation      |   |            |          |
| 5000 W. Chandler Blvd. |   |            |          |
| Chandler, AZ 85226     |   |            |          |
| Title                  |   |            |          |
| POWER CONNECTOR        |   |            |          |
| Size<br>A2             | Document Number<br>Intel® 815E Entry Appliance Platform | Rev<br>1.0 |          |
| Date                   | Tuesday, December 03, 2002                              | Sheet      | 28 of 33 |



NOTE:  
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT  
NO COMPONENTS PLACED FOR COMMUNICATIONS APPLIANCE

|   |   |            |
|---|---|------------|
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| Title<br>PS/2   |   |            |
| Size<br>A2  | Document Number<br>Intel® 815E Entry Appliance Platform | Rev<br>1.0 |
| Date:<br>Tuesday, December 03, 2002                               | Sheet<br>29   | of<br>33   |

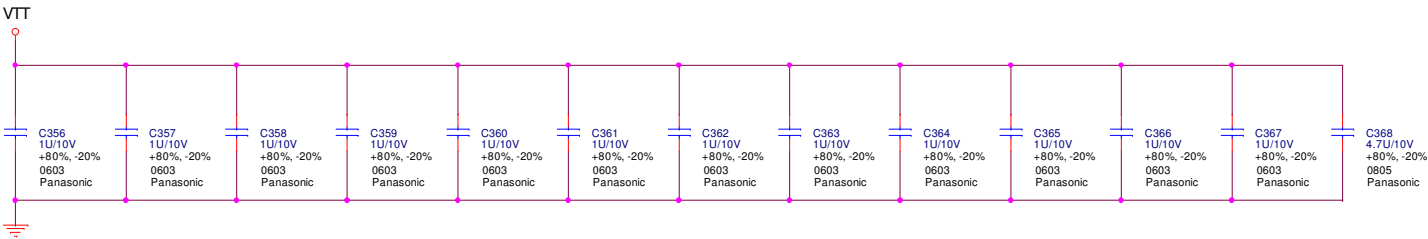




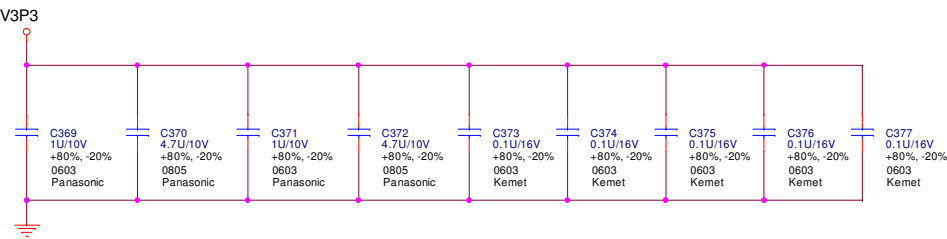
NOTE:  
PLACE ALL COMPONENTS FOR INTERACTIVE CLIENT  
NO COMPONENTS PLACED FOR COMMUNICATIONS APPLIANCE

|  |                                      |                |
|--|--------------------------------------|----------------|
| Intel Corporation                            |                                      |                |
| 5000 W. Chandler Blvd.<br>Chandler, AZ 85226 |                                      |                |
| Title  |                                      |                |
| AC97   |                                      |                |
| Size   | Document Number                      | Rev            |
| A2   | Intel® 815E Entry Appliance Platform | 1.0            |
| Date:  | Tuesday, December 03, 2002           | Sheet 31 of 33 |

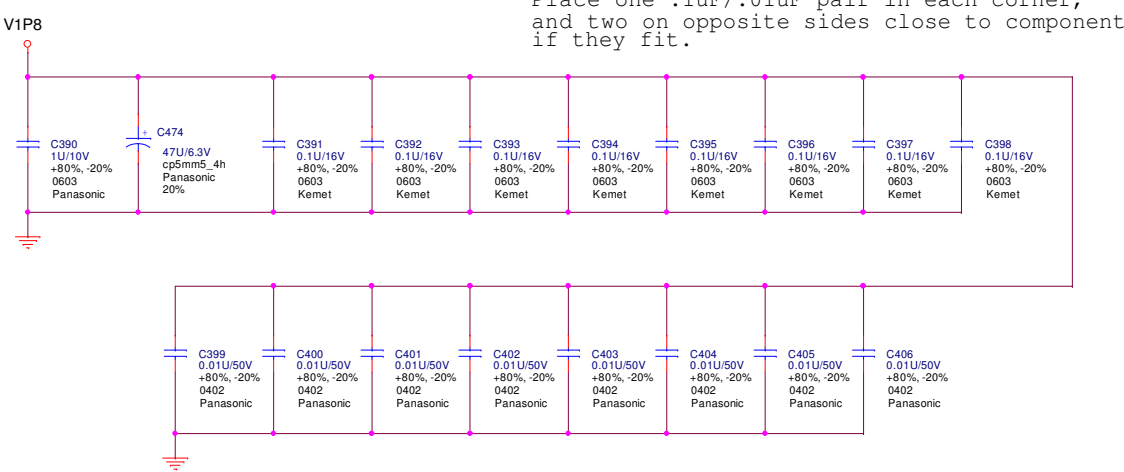
VTT Power Decoupling



Misc. Power Decoupling

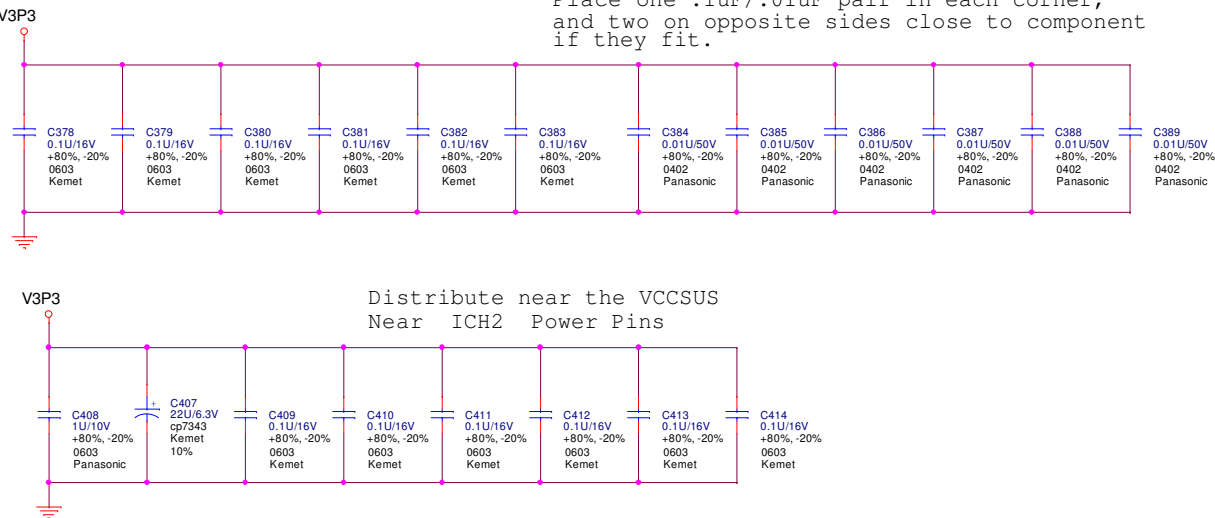


GMCH Decoupling



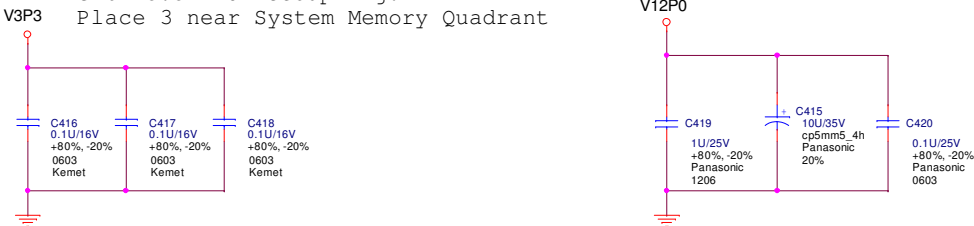
GMCH Core Plane Decoupling:  
Place one .1uF/.01uF pair in each corner,  
and two on opposite sides close to component  
if they fit.

ICH2 Decoupling

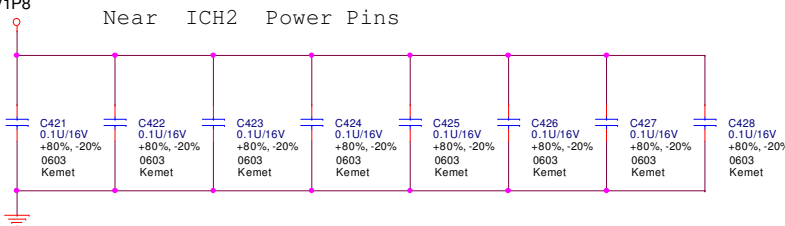


ICH2 3.3V Plane Decoupling:  
Place one .1uF/.01uF pair in each corner,  
and two on opposite sides close to component  
if they fit.

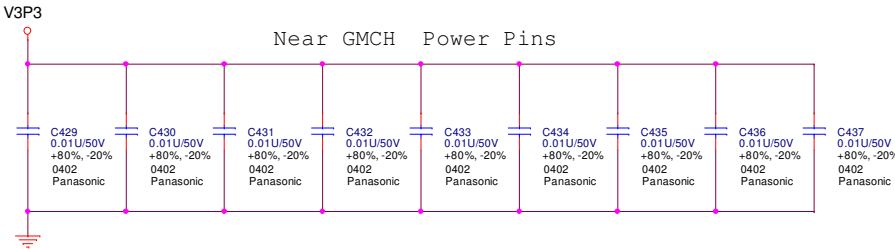
GMCH 3.3V IO Decoupling:  
Place 3 near System Memory Quadrant



Near ICH2 Power Pins

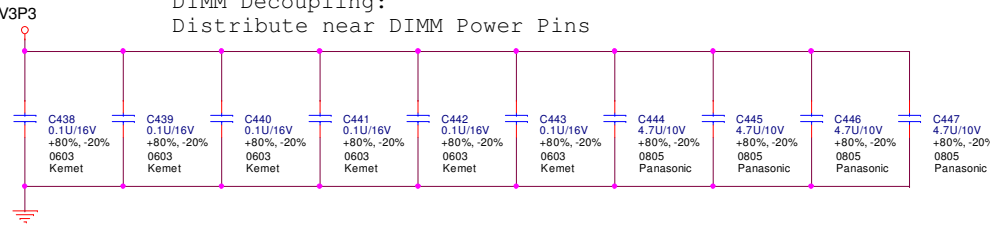


Near GMCH Power Pins

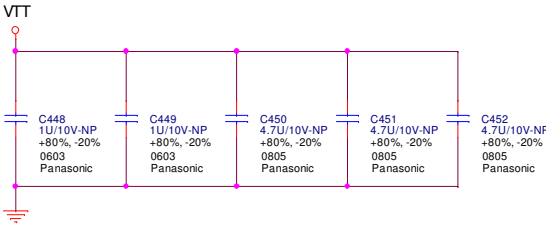


System Memory Decoupling

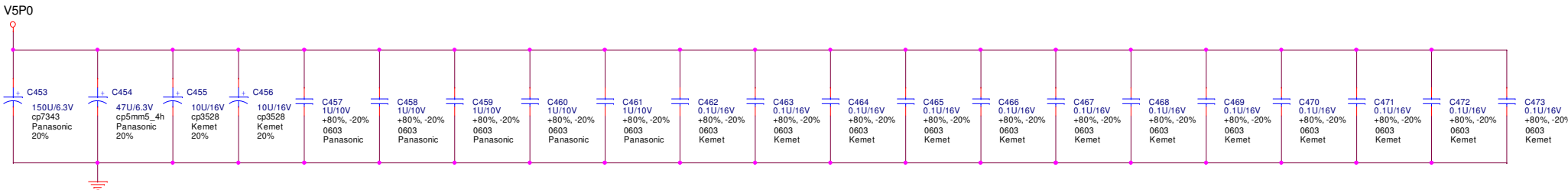
DIMM Decoupling:  
Distribute near DIMM Power Pins



VTT Power Decoupling



V5P0 Decoupling



NOTE:  
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|   |   |            |
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| Title<br>DECOUPLING   |   |            |
| Size<br>A2  | Document Number<br>Intel® 815E Entry Appliance Platform | Rev<br>1.0 |
| Date:<br>Tuesday, December 03, 2002                               | Sheet<br>32   | of<br>33   |



J1: ITP (15x2) Connector

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | Ground      | 2    | CPURST#     |
| 3    | Ground      | 4    | DBRESET#    |
| 5    | Ground      | 6    | TCK         |
| 7    | TDI         | 8    | TMS         |
| 9    | TDO         | 10   | VTT         |
| 11   | TRST#       | 12   | VTT         |
| 13   | N/C         | 14   | Ground      |
| 15   | PREQ#       | 16   | Ground      |
| 17   | PRDY#       | 18   | Ground      |
| 19   | N/C         | 20   | Ground      |
| 21   | N/C         | 22   | Ground      |
| 23   | N/C         | 24   | Ground      |
| 25   | N/C         | 26   | Ground      |
| 27   | N/C         | 28   | Ground      |
| 29   | N/C         | 30   | Ground      |

J2: VGA Board (6x2) Connector

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | VID_RED     | 2    | Ground      |
| 3    | VID_GREEN   | 4    | V1P8        |
| 5    | VID_BLUE    | 6    | Ground      |
| 7    | Ground      | 8    | 3VDDCDA     |
| 9    | 3VDDCCL     | 10   | CRT_HSYNC   |
| 11   | CRT_VSYNC   | 12   | V5P0        |

J3: FDC(17x2) Connector

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | Ground      | 2    | Density0#   |
| 3    | Ground      | 4    | N/C         |
| 5    | Ground      | 6    | Density1#   |
| 7    | Ground      | 8    | INDEX#      |
| 9    | Ground      | 10   | MOA#        |
| 11   | Ground      | 12   | DSB#        |
| 13   | Ground      | 14   | DSA#        |
| 15   | Ground      | 16   | MOB#        |
| 17   | Ground      | 18   | DIR#        |
| 19   | Ground      | 20   | STEP#       |
| 21   | Ground      | 22   | WD#         |
| 23   | Ground      | 24   | WE#         |
| 25   | Ground      | 26   | TRACK0#     |
| 27   | Ground      | 28   | WP#         |
| 29   | N/C         | 30   | RDATA#      |
| 31   | Ground      | 32   | HEAD#       |
| 33   | N/C         | 34   | DSKCHG#     |

J4: Tachometer FAN Connector

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | Ground             |
| 2          | V12P0              |
| 3          | Tachometer Signal  |

J5: PCI BUS CONNECTOR

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| B1   | N/C         | A1   | PTRST#      |
| B2   | PTCK        | A2   | V12P0       |
| B3   | Ground      | A3   | PTMS        |
| B4   | N/C         | A4   | PTDI        |
| B5   | V5P0        | A5   | V5P0        |
| B6   | V5P0        | A6   | PIRQ#B      |
| B7   | PIRQ#C      | A7   | PIRQ#D      |
| B8   | PIRQ#A      | A8   | V5P0        |
| B9   | N/C         | A9   | N/C         |
| B10  | N/C         | A10  | V5P0        |
| B11  | N/C         | A11  | N/C         |
| B12  | Ground      | A12  | Ground      |
| B13  | Ground      | A13  | Ground      |
| B14  | N/C         | A14  | N/C         |
| B15  | Ground      | A15  | PCIRST#     |
| B16  | PCICLK      | A16  | V5P0        |
| B17  | Ground      | A17  | PGNT#0      |
| B18  | PREQ#0      | A18  | Ground      |
| B19  | V5P0        | A19  | N/C         |
| B20  | AD31        | A20  | AD30        |
| B21  | AD29        | A21  | N/C         |
| B22  | Ground      | A22  | AD28        |
| B23  | AD27        | A23  | AD26        |
| B24  | AD25        | A24  | Ground      |
| B25  | N/C         | A25  | AD24        |
| B26  | C_BE#3      | A26  | IDSEL       |
| B27  | AD23        | A27  | N/C         |
| B28  | Ground      | A28  | AD22        |
| B29  | AD21        | A29  | AD20        |
| B30  | AD19        | A30  | Ground      |
| B31  | N/C         | A31  | AD18        |
| B32  | AD17        | A32  | AD16        |
| B33  | C_BE#2      | A33  | N/C         |
| B34  | Ground      | A34  | FRAME#      |
| B35  | IRDY#       | A35  | Ground      |
| B36  | N/C         | A36  | TRDY#       |
| B37  | DEVSEL#     | A37  | Ground      |
| B38  | Ground      | A38  | STOP#       |
| B39  | PLOCK#      | A39  | N/C         |
| B40  | PERR#       | A40  | SDONE       |
| B41  | N/C         | A41  | SBO#        |
| B42  | SERR#       | A42  | Ground      |
| B43  | N/C         | A43  | PAR         |
| B44  | C_BE#1      | A44  | AD15        |
| B45  | AD14        | A45  | N/C         |
| B46  | Ground      | A46  | AD13        |
| B47  | AD12        | A47  | AD11        |
| B48  | AD10        | A48  | Ground      |
| B49  | Ground      | A49  | AD9         |
|      | KEY         |      | KEY         |
|      | KEY         |      | KEY         |
| B52  | AD8         | A52  | C_BE#0      |
| B53  | AD7         | A53  | N/C         |
| B54  | N/C         | A54  | AD6         |
| B55  | AD5         | A55  | AD4         |
| B56  | AD3         | A56  | Ground      |
| B57  | Ground      | A57  | AD2         |
| B58  | AD1         | A58  | AD0         |
| B59  | V5P0        | A59  | V5P0        |
| B60  | ACK64#      | A60  | REQ64#      |
| B61  | V5P0        | A61  | V5P0        |
| B62  | V5P0        | A62  | V5P0        |

J6, J7: IDE Connectors (Sec=40, Pri=44)

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | RESET#      | 2    | Ground      |
| 3    | Data 7      | 4    | Data 8      |
| 5    | Data 6      | 6    | Data 9      |
| 7    | Data 5      | 8    | Data 10     |
| 9    | Data 4      | 10   | Data 11     |
| 11   | Data 3      | 12   | Data 12     |
| 13   | Data 2      | 14   | Data 13     |
| 15   | Data 1      | 16   | Data 14     |
| 17   | Data 0      | 18   | Data 15     |
| 19   | Ground      | 20   | V5P0        |
| 21   | DMAREQ      | 22   | Ground      |
| 23   | IOW#        | 24   | Ground      |
| 25   | IOR#        | 26   | Ground      |
| 27   | IOCHRDY     | 28   | Ground      |
| 29   | DMAACK#     | 30   | Ground      |
| 31   | IRQ15/14    | 32   | N/C         |
| 33   | SA1         | 34   | PDIAG#/CSEL |
| 35   | SA0         | 36   | SA2         |
| 37   | HDCCS0#     | 38   | HDCCS1#     |
| 39   | HDDACTIVE#  | 40   | Ground      |
| 41   | V3P3        | 42   | V3P3        |
| 43   | Ground      | 44   | N/C         |

J8: Dual USB Port Connector

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | 5VP0        | 5    | 5VP0        |
| 2    | USBD0-      | 6    | USBD1-      |
| 3    | USBD0+      | 7    | USBD1+      |
| 4    | Ground      | 8    | Ground      |

J9: Dual USB Header

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | PWR0        | 6    | D1+         |
| 2    | PWR1        | 7    | GND0        |
| 3    | D0-         | 8    | GND1        |
| 4    | D1-         | 9    | KEY         |
| 5    | D0+         | 10   | OC#         |

J10-A: VGA

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | RV          | 2    | GV          |
| 3    | BV          | 4    | MON2PU      |
| 5    | Ground      | 6    | Ground      |
| 7    | Ground      | 8    | Ground      |
| 9    | V5P0        | 10   | Ground      |
| 11   | MONOPU      | 12   | DDCDA       |
| 13   | HS          | 14   | VS          |
| 15   | DDCCL       |      |             |

J10B: Serial Port connector

D-SUB9 Male

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | DCD                |
| 2          | RXD                |
| 3          | TXD                |
| 4          | DTR                |
| 5          | SGND               |
| 6          | DSR                |
| 7          | RTS                |
| 8          | CTS                |
| 9          | RI                 |
| 10         | N/C ( J1 Only )    |

J11: Serial Port connector

2x5 Pin Header

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | DCD                |
| 2          | RXD                |
| 3          | TXD                |
| 4          | DTR                |
| 5          | SGND               |
| 6          | DSR                |
| 7          | RTS                |
| 8          | CTS                |
| 9          | RI                 |
| 10         | N/C ( J1 Only )    |

J12: DVO Connector

J13, J14: Ethernet RJ45 (8P8C) Connector

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | TX+         | 2    | TX-         |
| 3    | RX+         | 4    | Termplane   |
| 5    | Termplane   | 6    | RX-         |
| 7    | Termplane   | 8    | Termplane   |

J15: DC15V/5A Power Jack Connector

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | V15P0              |
| 2          | Ground             |
| 3          | Ground             |

J16: Reset push button (Momentary)

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | Reset signal       |
| 2          | Ground             |

J17: Power output connector to HDD

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | V12P0              |
| 2          | Ground             |
| 3          | Ground             |
| 4          | V5P0               |

J18: KB/Mouse

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | KDAT        | 2    | N/C         |
| 3    | Ground      | 4    | Ground      |
| 5    | KCLK        | 6    | N/C         |
| 7    | MDAT        | 8    | N/C         |
| 9    | Ground      | 10   | V5P0        |
| 11   | MCLK        | 12   | N/C         |
| 13   | Ground      | 14   | Ground      |
| 15   | Ground      | 16   | Ground      |
| 17   | Ground      |      |             |

J19-A: MIC

J19-B: Line In

J19-C: Headphone Out

J20: CD-ROM Audio

| Pin Number | Signal Description |
|------------|--------------------|
| 1          | Left In            |
| 2          | Ground In          |
| 3          | Ground In          |
| 4          | Right In           |

J21: Audio Planar

| P.N. | Description | P.N. | Description |
|------|-------------|------|-------------|
| 1    | Mic In      | 2    | GND Audio   |
| 3    | Mic Bias    | 4    | V5VAUD      |
| 5    | Out Right   | 6    | Ret Right   |
| 7    | RSVD        | 8    | KEY         |
| 9    | Out Left    | 10   | Ret Left    |
| 11   | Amp R+      | 12   | Amp R-      |
| 13   | Amp L+      | 14   | Amp L-      |

## JUMPER TABLE

| JUMPER Ref. | FUNCTION   | DEFAULT SETTING    |
|-------------|--|--------------------|
| JP1         | CLEAR CMOS RAM<br>1-2 : Normal<br>2-3 : CLEAR CMOS RAM   | 1-2 : Normal       |
| JP2         | CPU Frequency Strapping<br>IN : Force CPU Frequency to safe mode<br>OUT : Use CPU Frequency strapping in ICH2 Register | OUT : By ICH2 Reg. |
| JP3         | FWH Top Block LOCK<br>IN : TOP BLOCK UNLOCK<br>OUT : TOP BLOCK LOCK  | IN : UNLOCK        |
| JP4         | Ring Indicator Select<br>1-2 : RI Disconnected, External 12 V<br>2-3 : RI Connected                                    | 2-3 : RI Connected |
| JP5         | Ring Indicator Select<br>1-2 : RI Disconnected, External 12 V<br>2-3 : RI Connected                                    | 2-3 : RI Connected |

Intel Corporation

5000 W. Chandler Blvd.  
Chandler, AZ 85226

Title

REFERENCE TABLES

Size

A2

Document Number  
Intel® 815E Entry Appliance Platform

Rev

1.0

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